49th European Solid-State Device Research Conference

CONFERENCE PROGRAM

IEEE

ELECTRON DEVICES SOCIETY®
September 23-26, 2019
Kraków, Poland

ESSDERC

49th European Device Research Conference

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Since its inception in 1951, Rigaku has been at the forefront of analytical and industrial instrumentation technology. Today, with hundreds of major innovations to their credit, the Rigaku Group of Companies are world leaders in the fields of general X-ray diffraction (XRD), thin film analysis (XRF, XRD and XRR), X-ray fluorescence spectrometry (TXRF, EDXRF and WDXRF) and small angle X-ray scattering (SAXS). Rigaku in-line metrology systems lead with innovation, whether creating semiconductor chips or improving production line quality.

Single crystal X-ray diffractometers for chemical crystallography are developed and manufactured in Rigaku Polska sp. z o.o., a Rigaku group company in Poland. Rigaku also has state-of-the-art X-ray detectors with integrated circuits developed by AGH University of Science and Technology.

https://www.rigaku.com/
Xilinx develops highly flexible and adaptive processing platforms that enable rapid innovation across a variety of technologies – from the endpoint to the edge to the cloud. Xilinx is the inventor of the FPGA, hardware programmable SoCs and the ACAP (Adaptive Compute Acceleration Platform), designed to deliver the most dynamic processor technology in the industry and enable the adaptable, intelligent and connected world of the future in a multitude of markets including Data Center (Compute, Storage and Networking); Wireless/5G and Wired Communications; Automotive/ADAS; Emulation & Prototyping; Aerospace & Defense; Industrial Scientific & Medical, and others. Xilinx’s core strengths simultaneously address major industry trends including the explosion of data, heterogeneous computing after Moore’s Law, and the dawn of artificial intelligence (AI).

https://www.xilinx.com/

SK hynix has four production facilities in Wuxi and Chongqing, China as well as domestic business sites in Icheon and Cheongju. As a global company, SK hynix also operates sales subsidiaries in ten countries including the U.S., U.K., Germany, Singapore, Hong Kong, India, Japan, Taiwan and China, and four R&D corporate bodies in Italy, U.S., Taiwan and Belarus. Based on its 30-year-old know-how for production and operation of the semiconductor business, SK hynix makes efforts to secure competitiveness in technology and costs and lead the global semiconductor market by conducting continuous R&D activities and investment.

https://www.skhynix.com/eng/index.jsp
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Chair’s Message

On behalf of the entire Organizing Committee, it is our pleasure to welcome you to the 49th European Solid-State Device Research Conference (ESSDERC) and the 45th European Solid-State Circuits Conference (ESSCIRC) 2019. For the first time, ESSDERC and ESSCIRC take place in Cracow, Poland and the conferences are co-organized by AGH University of Science and Technology in Cracow, Jagiellonian University in Cracow, Warsaw University of Technology and Centre for Advanced Materials and Technologies CEZAMAT in Warsaw. Since 2003 both ESSDERC and ESSCIRC are running in parallel and have joint keynote speakers and joint focus sessions. The increasing level of integration for system-on-chip design made available by advances in semiconductor technology is calling for deeper interaction among technologists, device experts, IC designers and system designers. As a participant to ESSDERC and ESSCIRC, you not only have the opportunity to become familiar with the latest advances in these fields, but you will meet people who pioneered previous developments, you get access to enhance your international network in micro- and nano-electronics and you will be a witness to previews into emerging fields.

The conference takes place in Cracow – the city of Polish Kings. Cracow, being the capital of the Crown of the Kingdom of Poland between 1038 and 1569, it has never stopped thriving as an economic and cultural center. The uniqueness of this place has not gone unnoticed. Entire Cracow’s Historic Centre (Old Town) is on the UNESCO World Heritage List. It is recognized by many by its largest medieval market square in Europe and its architecture originating from Gothic through Renaissance and Baroque epochs. The Royal Wawel Castle, the seat of Polish kings and their biggest necropolis, is a diamond that rules over the landscape of the city. Another important feature of Cracow is its academical prowess. With over 650 years of academic tradition, it holds one of the oldest universities in Europe (Jagiellonian University). Currently, it is a home to five major universities (with AGH University of Science and Technology leading in engineering research) and various higher education school, which gives a total population of approximately 200 thousand students. The high-tech landscape in Cracow continues to expand. It boasts a special economic zone (Cracow Technological Park for major high-tech investments) with several major R&D centers focused on industrial electronics and software, four enterprise incubators, three commercial-fair grounds, and seven higher schools of economics. Over 100,000 private businesses and nearly 2,000 public firms carry on in Cracow with an aggregate revenue to the tune of 14.6 billion euro. Surprisingly, the city’s big companies with hundreds and thousands on the payroll come under the spotlight, yet they are hardly representative of Cracow’s economy. The self-employed and small enterprises employing less than ten workers account for over ninety percent of business entities incorporated in the city. Foreigners own (wholly or partially) more than 1,900 of Cracow’s companies. This year ESSDERC-ESSCIRC received a total of 345 submissions from 37 countries, of which 235 contributed to ESSCIRC, and 110 to ESSDERC submissions. About 56% of the submissions came from Europe, 24% from Asia, Pacific and 20% from North America, clearly demonstrating the international character of the conference. The conference has 4 plenary
keynote speakers coming from EPFL, Harvard University, Osaka University and STMicroelectronics, 3 ESSDERC plenary speakers coming from AIXTRON SE, Stanford University and Seoul National University and 3 ESSCIRC plenary speakers coming from TU Eindhoven, Tyndall National Institute and Intel. The selected papers are presented in 40 regular sessions. In collaboration with Important Project of Common European Interest (IPCEI) 3 additional focus sessions are organized. The program also includes extraordinary social program with a welcome reception and a conference banquet. These social events will offer ample opportunities for networking. Besides, the first day of the event on Monday, September 23rd will be dedicated to 7 tutorials (5 full-day tutorials and 2 full-day tutorials) and 1 SINANO workshop. These give extra opportunities for updating your knowledge of the state-of-the-art in the covered areas.

We thank the IEEE Solid-State Circuits Society (SSCS) and the IEEE Electron Devices Society (EDS) that are the official sponsors of ESSCIRC and ESSDERC, respectively. We also thank all external sponsors who have provided the additional support allowing us to offer the little extras that beyond doubt will make ESSDERC-ESSCIRC 2019 a memorable event in a long tradition.

We would also like to thank the Steering Committee of ESSDERC-ESSCIRC for giving us the opportunity to organize this event and for many valuable recommendations and discussions. We are very grateful to the excellent collaboration with the exceptional members of the Organizing Committee and the Technical Program Committee. All members have been extremely devoted and have worked very hard to make ESSDERC-ESSCIRC 2019 yet another successful event. Without their dedication, enthusiasm and professionalism, this would not have been possible. We also thank all collaborators and volunteers who have helped us out.

Finally, the real success of a conference is based on the support of all the authors who submitted papers to the conference and on the willingness of the keynote, invited, focus session and tutorial speakers to travel to Cracow and to share their knowledge and insights. Their support and efforts are highly appreciated. Enjoy the 2019 edition of ESSDERC-ESSCIRC and your visit to Cracow, Poland, and after enjoying and savoring this year’s program, we hope to see you all again in Grenoble, France, for ESSDERC-ESSCIRC 2020.

Pawel Grybos and Maciej Ogorzalek
Conference General Chairs – ESSDERC-ESSCIRC 2019

Tomasz Skotnicki and Romuald Beck
TPC Chairs – ESSDERC 2019

Bogdan Staszewski and Witold Pleskacz
TPC Chairs – ESSCIRC 2019
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Wieslaw Kuzmicz (WUT, PL) – TUTORIALS Co-Chair

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Christoph Sandner (Infineon, AT)
Michiel Steyaert (KU Leuven, BE)
Roland Thewes (TU Berlin, DE)
Akira Toriumi (Tokyo University, JP)
ESSDERC TECHNICAL PROGRAM COMMITTEE

TRACK 1 – Advanced CMOS: Process and Device Technology, Characterization and Reliability  
Nadine Collaert (Imec,BE)  Track Chair  
François Andrieu (CEA-LETI, FR)  
Maryline Bawedin (MINATEC, FR)  
Erik Bury (Imec, BE)  
Sorin Cristoloveanu (MINATEC, FR)  
Lukas Czornomaz (IBM Research Zürich, CH)  
Thanh Viet Dinh (NXP Semiconductors, BE)  
Blandine Duriez (TSMC, BE)  
Gabriella Ghidini (STMicroelectronics, IT)  
Jan Hoentschel (GlobalFoundries, DE)  
Hiroshi Iwai (Tokyo Institute of Technology, JP)  
Gunnar Malm (KTH Royal Institute of Technology, SE)  
Montserrat Nafria (UAB, ES)  
Jurriaan Schmitz (University of Twente, NL)  
Changhwan Shin (University of Seoul, KR)  
Shinichi Takagi (Tokyo Institute of Technology, JP)  
Yi Zhao (Zhejiang University, CN)  

TRACK 2 – Opto-, Power- and Microwave Devices  
Mikael Östling (KTH Royal Institute of Technology, SE)  Track Chair  
Denis Flandre (UC Louvain, BE)  Deputy Chair  
Dan Buca (Forschungszentrum Jülich, DE)  
Dana Cristea (IMT Bucharest, RO)  
Isodiana Crupi (CNR-IMM, IT)  
Wilfried Haensch (IBM T. J. Watson Research Center, US)  
Tetsu Kachi (Nagoya University, JP)  
Ekkanath Madathil (University of Sheffield, GB)  
Matteo Meneghini (University of Padova, IT)  
Peter Moens (ON Semiconductor, BE)  
Edwin Piner (Texas State University, US)  
Gianmauro Pozzovivo (Infineon, IT)  
Susanna Reggiani (University of Bologna, IT)  
Tetsuya Suemitsu (Tohoku University, JP)  
Florian Udrea (Cambridge University, GB)
TRACK 3 – Fundamental Physical Modeling of Materials and Devices

Denis Rideau (STMicroelectronics, FR)  Track Chair
Mathieu Luisier (ETH Zürich, CH)  Deputy Chair
Aryan Afzalian (Imec, BE)
El Mehdi Bazizi (AMAT, US)
Fabian Bufler (Imec, BE)
David Esseni (University of Udine, IT)
Ray Hueting (University of Twente, NL)
Juergen Lorenz (Fraunhofer, DE)
Bernd Meinerzhagen (TU Braunschweig, DE)
Victor Moroz (Synopsis, US)
Marco Pala (University Paris-Saclay, FR)
Massimo Rudan (University of Bologna, IT)
Viktor Sverdlov (TU Wien, AT)
Francois Triozon (CEA-LETI, FR)
Zlatan Stanojevic (GLOBAL TCAD Solutions, AT)
Enrico Sangiorgi (University of Bologna, IT)

TRACK 4 – Device and Circuit Compact Modeling

Daniel Tomaszewski (ITE Warsaw, PL)  Track Chair
Thierry Poiroux (CEA-LETI, FR)  Deputy Chair
Marco Bellini (ABB, CH)
Mansun Chan (Hong Kong University of Science and Technology, CN)
Merlyne De Souza (University of Sheffield, GB)
Wladek Grabinski (GMC, CH)
Benjamin Ifíñiguez (University Rovira i Virgili, ES)
Christophe Lallement (University of Strasbourg, FR)
Cristell Maneux (University of Bordeaux, FR)
Hisayo Momose (Yokohama University, JP)
Klaus-Willi Pieper (Infineon, DE)
Werner Posch (AMS, AT)
Sadayuki Yoshitomi (Toshiba, JP)
Jean-Michel Sallese (EPFL, CH)
Gilson Wirth (Federal Univ. of Rio Grande do Sul, BR)
Zhiping Yu (Tsinghua University, CN)
Xing Zhou (NTU, SG)
Santanu Mahapatra (IISC, India)
Yogesh Singh Chauhan (IIT Kanpur, India)
TRACK 5 – Advanced and Emerging Memories
Paolo Pavan (Univ. di Modena Reggio Emilia, IT)  Track Chair
Geoffrey Burr (IBM T.J. Watson Research Center, USA)
Sung-Woong Chung (SK Hynix, KR)
Jerome Dubois (XP, NL)
Ru Huang (Peking University, CN)
Franz Kreupl (TU München, DE)
Andrea Lacaita (Politecnico di Milano, IT)
Thomas Mikolajick (NaMLab and TU Dresden, DE)
Klaus Knobloch (Infineon, GE)
Innocenzo Tortorelli (Micron, US)
Elisa Vianello (CEA-LETI, FR)
Dirk Wouters (RWTH Aachen University, DE)
Kensuke Ota (Toshiba Memory Corp., JP)

TRACK 6 – MEMS, NEMS, Bio-sensors and Display Technologies
Mirjana Banjevic (Sensirion, CH)  Track Chair
Thomas Alava (CEA-LETI, FR)
Jens Anders (University of Stuttgart, DE)
Joachim Burghartz (IMS Stuttgart, DE)
Volker Cimalla (Fraunhofer, DE)
Montserrat Fernandez-Bolaños Badia (EPFL, CH)
Hoel Guerin (EPFL, CH)
Raluca Muller (IMT Bucharest, RO)
Debbie G. Senesky (Stanford University, US)
Radu Sporea (University of Surrey, GB)
Committees

TRACK 7 – Emerging non-CMOS Devices and Technologies

Max Lemme (RWTH Aachen University, AMO GmbHDE)  Track Chair
Jong-Hyun Ahn (Yonsei University, KR)
Cees de Groot (University of Southampton, GB)
Jean Pierre Colinge (CEA-LETI, FR)
Gianluca Fiori (University of Pisa, IT)
Elena Gnani (University of Bologna, IT)
Tibor Grasser (TU Wien, Austria)
Adrian Ionescu (EPFL, CH)
Ryoichi Ishihara (University of Delft, NL)
Siegfried Karg (IBM Research Zürich, CH)
Joachim Knoch (RWTH Aachen University, DE)
Heike Riel (IBM Research Zürich, CH)
Andreas Schenk (ETH Zürich, CH)
Hitoshi Wakabayashi (Tokyo Institute of Technology, JP)
Huili Grace Xing (Cornell University, US)
Thomas Zimmer (IMS Bordeaux, FR)
The magical city of Cracow is the second-largest city in Poland. Located in the south of the country on the Vistula river, it is a capital city of Lesser Poland Voivodeship. It is a place where history and tradition intertwine with culture, modern technologies, and economic development. Officially rooted in XIII\textsuperscript{th} century, its history is much older. Being the capital of the Crown of the Kingdom of Poland between 1038 and 1569, it has never stopped thriving as an economic and cultural center. Cracow's Golden Age came by the end of the 15th century when it was the thriving metropolis of a vast and prosperous kingdom stretching from the Black Sea to the Baltic Sea. The uniqueness of this place has not gone unnoticed. Entire Cracow's Historic Centre (Old Town) is on the UNESCO World Heritage List. It is recognized by many by its largest medieval market square in Europe and its architecture originating from Gothic through Renaissance and Baroque epochs. The Royal Wawel Castle, the seat of Polish kings and their biggest necropolis, is a diamond that rules over the landscape of the city. It was officially recognized as European Capital of Culture (2000), UNESCO City of Literature (2012) and hosted World Youth Days (2016) as well as participated in European Football Championship (2012). Another important feature of Cracow is its academic prowess. With over 650 years of academic tradition, it holds one of the oldest universities in Europe (Jagiellonian University). Currently, it is a home to five major universities (with AGH University of Science and Technology leading in engineering research) and various higher education school, which gives a total population of approximately 200 thousand students. The high-tech landscape in Cracow continues to expand. It boasts a special economic zone (Cracow Technological Park for major high-tech investments) with several major R&D centers (e.g. Motorola, ABB, Nokia, Aptiv, Silicon Creations, Ericsson, Comarch) focused on industrial electronics and software, four enterprise incubators, three
commercial fairgrounds, and seven higher schools of economics. Over 100,000 private businesses and nearly 2,000 public firms carry on in Cracow with an aggregate revenue to the tune of 14.6 billion euro. Surprisingly, the city’s big companies with hundreds and thousands on the payroll come under the spotlight, yet they are hardly representative of Cracow’s economy. The self-employed and small enterprises employing less than ten workers account for over ninety percent of business entities incorporated in the city. Foreigners own (wholly or partially) more than 1,900 of Cracow’s companies.
GETTING AROUND KRAKÓW!

Transportation in Kraków:
With most landmarks within easy walking distance from one another, the best way to enjoy old Kraków is on foot. The more so that the bulk of the city’s historic area has been turned into a pedestrian precinct. Although you can also roam the Old Town and Kazimierz historic districts driven in a horse cab, an electric cart with a taped guide, or a bicycle rickshaw. One may also take a tour of Kraków on a double-decker bus.

Public Transport in Kraków
Getting around in Kraków is pretty easy. There is no subway in Kraków, nonetheless this nearly million city has a fairly dense public transport system which consists of tramways and bus lines that mostly a municipal company operates and a number of private-owned minibus fleets. And some suburbanites commute by local trains.

When starting out on your trip, remember to stamp your ticket in our buses and trams. Ticket machines are available at all the main tram and bus stops. They are easy to use and provide entire range of tickets. You can buy tickets also on bus, trams from ticket machines, or drivers, but please note that often only coins are accepted. Some mobile apps enable buying tickets online (mPay, Mobilet and SkyCash).

Kraków’s Taxi Cabs
Taxicabs are plentiful and relatively inexpensive in Kraków. And you can dial roughly fifteen different taxi telephone centers, each with its own fleet. Do not expect an English speaker on the other end of the phone line but a cab will arrive in a few minutes to your address if you manage to give one. MayTaxi and UBER are available.

Recommended companies:
- Barbakan +48 12 19661
- Mega +48 12400 00 00
- iTaxi +48737737 737
CONFERENCE VENUE

Auditorium Maximum UJ
the conference center of the Jagiellonian University

address: ul. Krupnicza 33, 31-123 Kraków, Poland

The venue of ESSDERC/ESSCIRC 2019 Conferences is Auditorium Maximum, the conference center of the Jagiellonian University. The conference center is conveniently located right in the middle of Kraków, a 10-minute walk from the main square of Old Town. The building’s function and form are drawn from classical models worked out in the civilizations of the Mediterranean Sea basin. The main room is inspired by a Roman amphitheatre, in which the central figure was that of the speaker/actor and also allows for spectators’ mutual observation and interaction. Geometrical divisions of the facade, in turn, draw from the Greek temple with seven spaces in a colonnade. Yet this order is disturbed by the asymmetric division into two spaces forming the entrance zone. This results from the context and urbanistic order, with the building closing the perspective of Wenecja street. The entrance arcades surrounding the building serve as a meeting space for the academic circles. Plus, they act as a specific type of ‘threshold’ space, semi-private in contrast with the public character of street space. The main auditorium’s structure has been ‘rotated’ around a central spot to allow for arranging a ‘patio’. The centre, able to accommodate 1200 participants, offers also a complex of conference halls and support areas. Around the Centre, a special complex for transportation has been erected encompassing ground-level parking lots, a bus and minibus terminal and an area for mobile transmission units, as well as all underground parking.

Online view of Auditorium Maximum:
http://maximum.wkraj.pl/#/12557/0
SESSONS

• **SESSIONS, TUTORIALS, WORKSHOP** will take place in a Conference Venue, Auditorium Maximum.

• **REGISTRATION DESK**
  Registration Desk will be located close to the entrance of the conference venue.

• **LUNCHES**
  Lunches will be served in the conference venue foyer (Monday) or in the Exhibition Room (Tuesday – Thursday).

• **SSCS DIVERSITY LUNCHEON: CULTIVATING ENGINEERING CONFIDENCE**
  Tuesday, September 24, 12:40 pm – 2:00 pm. Bistro Room (level 0)
  Please pick up lunch and bring it along. Drinks, coffee and dessert will be provided.
  The luncheon will feature talks by industry and academic professionals sharing their experience in their careers where a challenge, a project or a mentor helped them becoming a better engineer and problem solver. We will follow on with a group discussion around mentoring and sponsorship best practices.
  *Sponsored by the IEEE Solid-State Circuits Society*

• **YOUNG PROFESSIONALS AND STUDENTS MICRO-MENTORING AND CAREER COACHING SESSION**
  Monday, September 23, 6:30 pm – 8:00 pm.
  Exhibition Room (level 2)
  Leading experts from industry and academia, IEEE SSCS Executives, and Distinguished Leaders will share their experiences. Registration is required.
  *Sponsored by the IEEE Solid-State Circuits Society and the IEEE Young Professionals*

• **SSCS CHAPTER CHAIRS MEETING**
  Wednesday, September 25, 2:20 pm – 4:20 pm.
  Conference Room (level 2).
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<th>Monday September 23, 2019 — Tutorials, Workshop</th>
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<td>Main Auditorium A</td>
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<tr>
<td>Registration</td>
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<tr>
<td>08:00 – 08:30</td>
<td>Tutorials</td>
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<tr>
<td>08:30 – 10:00</td>
<td>Morning Session I</td>
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<tr>
<td>10:00 – 10:30</td>
<td>Morning Session II</td>
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<tr>
<td>10:30 – 12:00</td>
<td>Lunch</td>
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<tr>
<td>15:30 – 16:00</td>
<td>Lunch</td>
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<td>16:00 – 18:30</td>
<td>Afternoon Session I</td>
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<tr>
<td>18:30 –</td>
<td>Young Professionals and Students Micro-Mentoring and Career Coaching Session (Exhibition Room)</td>
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Legend:
- Tutorials
- Workshop
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<thead>
<tr>
<th>Time</th>
<th>Room</th>
<th>Main Auditorium A</th>
<th>Main Auditorium B</th>
<th>Small Aula</th>
<th>Conference Room</th>
<th>Medium Aula A</th>
<th>Medium Aula B</th>
<th>Seminar Room</th>
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<tr>
<td>08:00 – 08:30</td>
<td>Registration</td>
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<td>08:30 – 09:00</td>
<td>Auditorium A and B: Conference Opening and Welcome</td>
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<td>09:00 – 09:40</td>
<td>Joint Plenary 1: Edoardo Charbon, EPFL, Cryo-CMO S: 60 Years of Technological Advances towards Emerging Quantum Technologies</td>
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<td>10:20 – 11:00</td>
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<td>11:00 – 12:20</td>
<td>Analog Techniques</td>
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<td>12:20 – 14:00</td>
<td>Lunch</td>
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<td>Auditorium A and B: Joint Plenary 3: Toshio Yanagida, Osaka University, Single Molecule Nano-Science: Noise and Function of Life</td>
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<td>10:20 – 12:00</td>
<td>High Resolution SAR ADC</td>
<td>Wireless RX</td>
<td>MM-Wave Frequency Multipliers</td>
<td>Machine Learning and Accelerators</td>
<td>Advanced and Emerging Memories</td>
<td>Non-Conventional Devices</td>
<td>Modeling of Compound Semiconductor Devices</td>
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<td>14:20 – 15:40</td>
<td>Amplifiers and Filters</td>
<td>Wireline</td>
<td>Power Management</td>
<td>SSCS Chapter Chairs Meeting</td>
<td>Analog/RF</td>
<td>Hardware for Neuromorphic Computing</td>
<td>Advances in MOSFET Modeling</td>
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<td>Bus Departure to Wieliczka Salt Mine – Gala Dinner</td>
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<td>Auditorium A and B: Joint Plenary 4: Donhee Ham, Harvard University. Copying Brain with Semiconductor Technology</td>
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<td>10:20 – 12:00</td>
<td>High-Speed ADC</td>
<td>Sensor Interfaces</td>
<td>Millimeter-wave Power Amplifiers</td>
<td>Memory-Centric Design</td>
<td>Modeling of Trap Effects and Noise</td>
<td>Photonic and Microwave Devices</td>
<td>Multi-physics Modeling</td>
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<td>14:20 – 15:40</td>
<td>Sigma-Delta and Time-Based ADC</td>
<td>Wireless TX</td>
<td>RX and Imaging Techniques</td>
<td>Derivative Technologies</td>
<td>Optical and Thermal Sensors</td>
<td>Advanced Device Modeling</td>
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Language
The official language of the conference is English: no simultaneous translation will be available.

Badges
Badges must always be visibly worn during the scientific session, coffee breaks, and lunches at the conference site but also during social program activities.

Internet / Wi-Fi
Wi-Fi connection will be available on site.

Certificate of Attendance
Certificates will be available on-site for all registered participants.

Time Zone
Poland and Kraków are located in the Central European Standard time zone CET (GMT + 1 hour)

Language in Poland
The official language is Polish.

Climate
The climate in Poland is moderate continental with four seasons. September has an average temperature of 14°C with evening lows of 9°C. In the afternoon, temperatures peak at 19°C and chances of rain.

Currency
The official Polish currency is the “złoty” (PLN). Money may be exchanged at all banks as well as at authorized exchange offices. Złoty current exchange rate may be checked on the website of the National Bank of Poland (http://www.nbp.pl/homen.aspx?f=/srodeken.htm). Banks are open approximately from 8:00 until 18:00 Monday through Friday.

Credit Cards
ATMs are located throughout the city and accept most major credit cards (Visa, Master Card, Maestro, American Express, Diners, Cirrus etc.). Major credit cards are accepted at almost all restaurants and businesses in Poland.
TELEPHONE CALLS
The country code for Poland is +48 and the Kraków code is (12). For international calls, please dial the International Access Code 00 or +. Mobile operators in Poland: T-mobile, Orange, Play, Plus.

ELECTRICITY
Electricity in Poland is 230 V, 50 Hz. Electrical outlets are standard European. For 110 V, 60 Hz appliances, you will need an adapter plug, and may also need a converter.

COFFEE BREAKS AND LUNCHES
Coffee breaks and lunches will be served free of charges at the Conference to fully registered participants wearing their badges. Accompanying Persons have no access to scientific sessions, coffee breaks or lunches. Please note that vegetarian dishes will be on the daily menu; for other special needs, we will try to serve a good variety of food so that it will be easier for you to get some alternatives in case of special diet restriction.

SMOKING POLICY
Participants are requested to refrain from smoking inside the venue.

PEOPLE WITH SPECIAL NEEDS
Every effort has been made to ensure that people with special needs are catered for during the Conference. Should you require any specific assistance, please let us know in advance to enable to assist in making your stay at the Conference pleasant and comfortable; the conference secretariat and the conference chair can be contacted any time during the event of in advance via the official secretariat contacts.

EMERGENCY CALLS
112 is an international number for emergency calls.

CONTACT TO THE CONFERENCE SECRETARIAT
Foundation for AGH University of Science and Technology
ul. Czarnowiejska 50B, 30-054 Kraków, Poland
Phone: +48 504 004 517, +48 664 242 650
Email: kf@agh.edu.pl

LOCAL SCIENTIFIC SECRETARIAT
Krzysztof Kasiński (AGH UST, PL)
Robert Szczygiel (AGH UST, PL)
WELCOME COCKTAIL (TUESDAY)
AGH University of Science and Technology in Cracow – the Main Building A0

We would like to kindly invite you to take part in Welcome Cocktail on September 24th 2019. Time: 7 pm.
Location: av. Mickiewicza 30, 30-059 Kraków (400m from Auditorium Maximum)
GALA DINNER (WEDNESDAY)
WIELICZKA SALT MINE

The Conference Gala Dinner will take place on September 25th 2019, deep underground in Wieliczka Salt Mine, Warszawa Chamber. Bus transportation will be arranged from the conference venue (4:00 pm – 4:10 pm).

UNESCO List of World Cultural Heritage – one of the oldest salt mines in Europe. Magnificent chambers chiseled out in rock salt. Amazing underground saline lakes, majestic timber constructions and unique statues sculpted in salt. Almost 3 kilometers of meandering corridors at a depth of 135 meters underground.

Important information

- Persons with mobility problems should be aware that the tour takes about 1 hour, and there are 800 steps in total of which 350 have to be descended at the beginning.
- Only limited part of the route is adapted for wheelchairs. Wheelchair width is limited to 59 centimeters. All disabled persons who want to join the Conference Tour are kindly asked to contact the organizers in advance.
- People who suffer from claustrophobia or chronic illness should seek medical advice before going underground.
- Please bring warm clothing and comfortable shoes. Temperature underground ranges between 14° and 16° C and the tour of the mine takes about 1 hour.
- Two toilet facilities are spaced along the route, 40 and 90 minutes from the beginning respectively.
- Smoking and using an open fire in the mine is strictly prohibited.

Wieliczka Salt Mine, Danilowicz Shaft
Danilowicz St. 10, 32-020 Wieliczka
www.wieliczka-saltmine.com
SIGHTSEEING KRAKÓW – CITY TOUR
(SUNDAY, OPTIONAL)

September 22nd, Sunday
Time: 6.30 p.m.

Kraków Sightseeing

Kraków is one of the oldest and most beautiful cities in Central Europe, chosen as the European City of Culture 2000. The Old Town of Kraków was entered on the UNESCO World Cultural Heritage List. Kraków has a unique charm, created by centuries of history and cultural wealth. It is not a simple task to describe the unique character of Kraków to those who still have not had the opportunity to visit this city. This uniqueness is primarily due to the rare cultural heritage embodied within the city walls. Here, in the year 1000, a Roman Catholic bishopric was founded. Here, the residential royal castle was constructed on the Wawel Hill, becoming the site for the coronations and burials of kings, as Kraków was the capital of Poland from the 11th to 17th century. Here in 1364, the Kraków Academy was established, the first Polish University (today renamed the Jagiellonian University).

Sightseeing time: Approximately 2-3 hrs
If you are interested in taking part in city tours, please book a place on-line through your ESSDERC/ESSCIRC 2019 registration account. Additional cost: 35 EUR
KRAKÓW EVENING TOUR
(MONDAY, OPTIONAL)

September 23rd, Monday
Time: 6.30 p.m. – 9.00 p.m.

See all the highlights of the Old Town area that made Cracow so famous. Starting with Barbican – the remaining fragments of city fortifications, the masterpiece of medieval military structures built in the 15th century. The spectacular Main Market Square with the Renaissance Cloth Hall – a perfect place to buy local souvenirs, the Town Hall Tower and St Mary’s Basilica with a unique wooden masterpiece of Veit Stoss. Don’t miss the buildings of Poland’s oldest university, Jagiellonian University, where Nicolaus Copernicus studied. Wawel Hill that is dominated by the Cathedral, the Castle and the defense towers. Wawel Cathedral used to be the scene of coronations and is the eternal resting place of the kings of Poland.

Sightseeing time: Approximately 2-3 hrs
If you are interested in taking part in city tours, please book a place on-line through your ESSDERC/ESSCIRC 2019 registration account. Additional cost: 35 EUR
GENERAL PURPOSE OF THE CONFERENCE

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The increasing level of integration for system-on-chip design made available by advances in semiconductor technology is, more than ever before, calling for deeper interaction among technologists, device experts, IC designers, and system designers. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

ESSDERC 2019 TRACKS:

- CMOS Devices and Technology
- Opto-, Power and Microwave Devices
- Physical Modeling of Materials and Devices
- Compact Modeling of Devices and Circuits
- Memory Devices and Technology
- Sensor Devices and Technology
- Emerging non-CMOS Devices and Technologies

FOCUS TRACKS:

- Challenges for Power Devices & Merging Microelectronics with Optics
- MEMS, Sensors & Advanced Integration Technologies
- Advanced Semiconductor Process & Device Technologies in Europe
Abstract: Quantum technologies hold the promise to address intractable computing, communication, and sensing problems by exploiting quantum physics concepts, such as superposition and entanglement. Let us consider a quantum computer, its core being the qubit, which requires classical control electronics, possibly in close proximity. Qubits live at deep-cryogenic temperatures and thus any control electronics should be fully operational at a similar temperature. In this context a new field of engineering is emerging aimed at the creation of cryogenic CMOS (cryo-CMOS) circuits and systems optimized for low-Kelvin operation. Leveraging the advances of the last 60 years in integrated electronics and Moore’s Law, new modeling and circuit techniques, system-level methodologies and design automation are blossoming, often involving knowledge creation and/or renewal. In this talk, we will outline the challenges of modeling, designing, testing, and operating complex circuits and systems at 4 Kelvin and below. We will discuss preliminary results achieved in the control and read-out of qubits by ad hoc integrated circuits optimized for low power and cryogenic operation. The talk will conclude with a perspective on the field and its trends.

Edoardo Charbon (SM’00 F’17) received the Diploma from ETH Zurich, the M.S. from the University of California at San Diego, and the Ph.D. from the University of California at Berkeley in 1988, 1991, and 1995, respectively, all in electrical engineering and EECS. He has consulted with numerous organizations, including Bosch, X-Fabs, Texas Instruments, Maxim, Sony, Agilent, and the Carlyle Group. He was with Cadence Design Systems from 1995 to 2000, where he was the architect of the company’s initiative on information hiding for intellectual property protection. In 2000, he joined Canesta Inc., as the Chief Architect, where he led the development of wireless 3-D CMOS image sensors. Since 2002 he has been a member of the faculty of EPFL, where is a full professor since 2015. From 2008 to 2016 he was with Delft University of Technology’s as Chair of VLSI design. He has been the driving force behind the creation of deep-submicron CMOS SPAD technology, which is mass-produced since 2015 and is present in smartphones, telemeters, proximity sensors, and medical diagnostics tools. He has also been the strong proponent of using cryogenic CMOS (cryo-CMOS) circuits and systems for the classical control of quantum processors, so as to achieve scalable quantum computers. His interests span from 3-D vision, FLIM, FCS, NIROT to super-resolution microscopy, time-resolved Raman spectroscopy, and cryo-CMOS circuits and systems for quantum computing. He has authored or co-authored over 350 papers and two books, and he holds 21 patents. Dr. Charbon is a distinguished visiting scholar of the W. M. Keck Institute for Space at Caltech, a distinguished lecturer of the IEEE Photonics Society, a fellow of the Kavli Institute of Nanoscience Delft, and a fellow of the IEEE.
Abstract: Massively parallel, intracellular recording of a large number of mammalian neurons across a network has been greatly desired in neurobiology, but it has proven very difficult to achieve. For instance, the intracellular recording by the patch clamp electrode boasts unparalleled sensitivity that can measure down to synaptic events, but it is too bulky to be implemented into a dense massive-scale array, and thus far only ~10 parallel patch recordings have been possible. Optical methods—e.g., voltage-sensitive dyes/proteins—have been developed in hopes of parallelizing intracellular recording, but they have not been able to perform recording from more than ~30 neurons in parallel. As an opposite example, the microelectrode array (MEA) can record from far more neurons, but this extracellular technique has too low a sensitivity to tap into synaptic activities. In this talk, I would like to share our on-going effort, the development of a CMOS chip that massively parallelizes intracellular recording from a large number of mammalian neurons forming a network, and its applications in functional connectome mapping, high-throughput electrophysiological screening of drugs, and copying biological neuronal network for machine intelligence, where the last example will be a particularly important focus of the presentation.

Donhee Ham (http://ham.seas.harvard.edu) is Gordon McKay Professor of Applied Physics and EE at Harvard. He earned a B.S. degree in physics from Seoul National University. Following a 1.5-year military service in South Korea, he went to Caltech for graduate training in physics. There he worked in LIGO under Professor Barry Barish while in physics and later obtained a Ph.D. in EE winning the Wilts Prize for the best EE thesis. The intellectual focus of his group at Harvard is on the neuro-electronic interface, NMR biomolecular spectroscopy, integrated circuits, and quantum and low-dimensional devices.
Abstract: Since biological molecular machines such as molecular motors, cell signal processors, DNA transcription processors and protein synthesizers are only nanometers in size and have a flexible structure, they are very prone to thermal agitation. Furthermore, the input energy level is not much different from that of average thermal energy, kBT. Molecular machines can use this thermal noise with a high efficiency of energy conversion for their functions. This is in sharp contrast to man-made machines that operate at energies much higher than thermal noise. In recent years, single molecule imaging and nano-technologies have rapidly been expanding to include a wide range of life science applications. The dynamic properties of biomolecules and the unique operations of molecular machines, which were previously hidden in averaged ensemble measurements, are now being unveiled. The aim of our research is to approach the engineering principle of adaptive biological systems by uncovering the unique operation of biological molecular machines. Here, I review our single molecule experiments designed to investigate molecular motors, enzyme reactions, protein dynamics and cell signaling, and discuss how thermal fluctuations (noise) play a positive role in the unique operation of biological molecular machines allowing for flexible and adaptive biological systems including cell and brain.

Bio: Toshio Yanagida was born in Hyogo prefecture in 1946. He graduated from Osaka University and received the Doctor of Engineering degree in 1976. He was a Professor at Osaka University’s Graduate School of Information Science and Technology from 1988, Department of Physiology and Biosignaling, Graduate School of Medicine from 1996, and the Graduate School of Frontier Biosciences from 2002. His research was grounded by the development of pioneering new single molecule detection techniques, which allowed him to make fundamental discoveries on the molecular mechanisms of muscle contraction, and the role of fluctuation in the function of bio molecular machine. In his later research, he has extended the core idea of fluctuation mechanisms from molecular motors to cells and brain. He worked as the leader of the Yanagida Biomotron Project, ERATO, JST from 1992 to 1997 and its successor, the Single Molecule Process Project, ICORP, JST from 1998 to 2002. Following these projects, he was Research Director of Soft Nano Machines and Research Supervisor of Novel Measuring and Analytical Technology Contributions to the Elucidation and Application of Life Phenomena, CREST, JST from 2004 to 2012. From 2004 to 2006, he was Vice-Chair of the Council of Scientists of The International Human Frontier Science Program Organization, and from 2006 to 2010, he served as a Member of Council of the Biophysical Society. More recently, he has served as Director of the RIKEN Quantitative Biology Center (QBIC), and is currently Director of the Center for Information and Neural Networks (CiNet), NICT, while also holding the titles of Specially Appointed Professor, Osaka University, and Director, NEC Brain-Inspired Computing Research Alliance Laboratories. He has received a number of prestigious awards including the Imperial Prize and Japan Academy Prize in 1998, the US Genomic Award for Outstanding Investigator in the Field of Single Molecule Fluorescence Microscopy in 2010, and Fellow of the US Biophysical Society 2011. He was also honored as a Person of Cultural merit by the Emperor of Japan in 2013.
**Abstract:** The era of future applications in the field of the internet of things or the advanced automotive will require very complex System on Chip (SoC) co-integrating key elements such as high speed digital at low voltage, high-performance RF and analog devices with embedded fast non-volatile memories. The integration of those advanced ingredients will face two major constraints: being cost-effective and fully reliable. In order to fulfill suitably the performance level expected by applications without any compromise for cost and reliability, we propose a dedicated technology merging the 28FD-SOI solution with a Phase Change Memory (PCM) architecture. In this joint keynote, we will present this technology focusing first on the advantages in term of low voltage operation and devices variability reduction brought by body biasing. Superior analog behavior will be discussed by evidencing performance enhancement on usual design blocks. Finally, embedded PCM scheme will be presented showing reliability results compatible with automotive grade-0 criteria.

**Franck Arnaud** joined STMicroelectronics in 1995 after his graduation for a Master degree in the field of electronics from the Superior School of Electricity, so-called Sup’Elic from Paris university. He started the ramp-up of 0.35um CMOS technology as FEOL and device engineer. In 2008, he spent three years in Fishkill area working in ISDA semi-conductor alliance led by IBM as 32/28nm device manager. He moved back to Crolles site in France in 2010 where he took the responsibility of the 28nm program development for both bulk and FDSOI technologies as director. Since 2016, he is driving the development phase of 28FDSOI-ePCM technology in Crolles site.
Abstract: Wide band-gap semiconductors such as GaN and related materials are making inroads into power electronics applications realizing a significant power efficiency gain over Silicon based solutions. The automotive industry is an important use example for an accelerated adoption of these next generation semiconductor materials. The next generation mobile communication standard 5G utilizes the outstanding material properties of GaN to enable higher data rates and several more advantages. Employed in traction inverters of battery electric vehicles GaN based circuits lead to longer driving range or reduction of battery size for system cost optimization. GaN based AC-DC on-board chargers can be designed with a smaller factor when operating at higher switching frequencies due to smaller passive components and reduced cooling efforts. Charging infrastructure is upgraded with DC charging poles of several 100 kW of power to allow for faster direct charging of the vehicle battery which is expected to greatly improve consumer adoption. Therefore, the wide bandgap semiconductor content, in particular SiC or GaN, in next generation automotive applications will be growing strongly, which is resulting in investments into wide bandgap material supply chain and device manufacturing capabilities worldwide. This market demand drives our present epitaxial production roadmap as discussed here. The focus of epitaxy production technology developments has been put on productivity enhancements concepts like wafer level automation, in-situ metrology to acquire process data for smart system control and predictive maintenance concepts. The requirements for the process equipment are multifold, demanding utmost control of dopant and layer thickness uniformity and low defect density of the epitaxial layers. Besides layer quality, the ability to manufacture the device layer stacks reproducibly and economically is crucial to support the growing demand. Employing cassette-to-cassette wafer loading leads to a drastic reduction of process cycle time of up to 50% through hot wafer loading. By designing in an optical path to the growing wafer surface we have succeeded in establishing emissivity corrected pyrometry for on-wafer temperature measurement. This metrology enables wafer level control for process and epi yield optimization as well as for introduction of smart system concepts. Using a gas driven wafer carrier (satellite) rotation the surface temperature of each wafer can be tracked individually and can be adjusted by an N2/H2 gas mixture for temperature uniformity control during the process. A software based automatic correction of the gas flow to the individual satellites minimizes the mean surface temperature deviation of each wafer for each process step. We will report on the benefits of this technology to the optimization of epi layer properties like mean thickness and doping concentration within an 5×200 mm process run. GaN on Silicon for power and RF applications has demonstrated technological maturity. Rather the economical rational of how to improve cost efficiency in
the material and device production is considered to be the obstacle for the faster adoption today. We will present our recent work performed in a G5+ C Planetary Reactor® for high volume manufacturing of GaN-based devices on 150 or 200 mm Si. To achieve high buffer breakdown voltages up to 1kV and low dispersion, suitable buffer technologies, as well as carbon doping schemes, will be discussed.

Prof. Dr. Michael Hecken was born in Oberhausen, Germany on November 17, 1961. He received the Diplom-Ingenieur degree and the Dr.-Ing. degree in Electrical Engineering from Duisburg University in 1985 and 1989, respectively. He joined the Institut für Halbleitertechnik at RWTH Aachen as a senior engineer and has been working in the field of metalorganic vapor phase epitaxy for electronic and optoelectronic devices. In 1994 he finished his Habilitation in semiconductor technology and devices with a thesis on MOCVD technology for optoelectronic devices. Since then and still at present he has been a lecturer for semiconductor technology and devices as well as circuits for communication systems at RWTH. In 1997 he joined AIXTRON SE in Aachen-Germany where he is now Vice President Corporate Research & Development. In 1999 he was honored as Professor at RWTH Aachen. His main experience is in the fields of semiconductor growth by MOVPE, Nanotechnology, electronic and optoelectronic devices and circuits.

Prof. Hecken is author and co-author of more than 650 publications in international journals and several invited papers at international conferences. He was President of DGKK (German Crystal Growth Association), he is elected Executive Committee member of the IOCG (International Organization of Crystal Growth), member of VDE/ITG and was a board member of OptechNet e.V. and EPIC. He acts as a referee for international Journals. He has been granted several patents in the field of semiconductor technology. More than 250 publically funded projects were successfully managed by Professor Hecken.
Subhasish Mitra  
Stanford University, US

The N3XT 1,000X for the Coming Superstorm of Abundant Data: Carbon Nanotube FETs, Resistive RAM, Monolithic 3D

Abstract:
The world’s appetite for analyzing massive amounts of data is growing dramatically. The computation demands of these abundant-data applications, such as machine learning, far exceed the capabilities of today’s computing systems, and can no longer be met by isolated improvements in transistor technologies, memories or integrated circuit architectures alone. To achieve unprecedented functionality, speed, and energy efficiency, one must create transformative NanoSystems which exploit unique properties of underlying nanotechnologies to implement new architectures. This talk will present the N3XT (Nano-Engineered Computing Systems Technology) approach that enables such NanoSystems through: (i) new computing system architectures leveraging emerging device (logic and memory) nanotechnologies and their dense 3D integration with fine-grained connectivity for computation immersed in memory, (ii) new logic devices (carbon nanotube field-effect transistors for implementing high-speed and low-energy logic circuits) as well as high-density non-volatile memory (resistive RAM), amenable to (iii) ultra-dense (monolithic) 3D integration of thin layers of logic and memory devices that are fabricated at low temperature. A wide variety of N3XT hardware prototypes represent leading examples of transforming scientifically-interesting nanomaterials and nanodevices into actual NanoSystems. N3XT NanoSystems target 1,000X system-level energy-delay product benefits especially for abundant-data applications. Such massive benefits enable a broad range of applications that push new frontiers, from deeply-embedded computing systems all the way to the cloud.

Bio:
Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University. He directs the Stanford Robust Systems Group, co-leads the Computation focus area of the Stanford SystemX Alliance, and is a faculty member of the Wu Tsai Neurosciences Institute. Prof. Mitra also holds the Carnot Chair of Excellence in NanoSystems at CEA-LETI in Grenoble, France. His research ranges across robust computing, NanoSystems, Electronic Design Automation, and neurosciences. Results from his research group have been widely deployed by industry and have inspired significant development efforts by government and research organizations in multiple countries.
Jointly with his students and collaborators, Prof. Mitra demonstrated the first carbon nanotube computer and the first three-dimensional NanoSystem with computation immersed in data storage. These demonstrations received widespread recognition: cover of NATURE, Research Highlight to the United States Congress by the National Science Foundation, and highlight as “important, scientific breakthrough” by news organizations around the world.
In the field of robust computing, Prof. Mitra and his students created key approaches for soft error resilience, circuit failure prediction, on-line self-test and diagnostics, and QED (Quick Error Detection) design verification and system validation. His earlier work on X-Compact test compression at Intel Corporation has proven essential to cost-effective manufacturing and high-quality testing of almost all electronic systems across the industry. X-Compact and its derivatives have been implemented in widely-used commercial Electronic Design Automation tools.

Prof. Mitra’s honors include the ACM SIGDA / IEEE CEDA Newton Technical Impact Award in Electronic Design Automation (a test of time honor), the Semiconductor Research Corporation’s Technical Excellence Award (for innovation that significantly enhances the semiconductor industry), the Intel Achievement Award (Intel’s highest corporate honor), and the United States Presidential Early Career Award for Scientists and Engineers from the White House. He and his students have published award-winning papers at major venues: ACM/IEEE Design Automation Conference, IEEE International Solid-State Circuits Conference, ACM/IEEE International Conference on Computer-Aided Design, IEEE International Test Conference, IEEE Transactions on CAD, IEEE VLSI Test Symposium, and the Symposium on VLSI Technology. At Stanford, he has been honored several times by graduating seniors “for being important to them during their time at Stanford.”

Prof. Mitra has served on the Defense Advanced Research Projects Agency’s (DARPA) Information Science and Technology Board as an invited member. He is a Fellow of the Association for Computing Machinery (ACM) and the Institute of Electrical and Electronics Engineers (IEEE).
Abstract:
Artificial intelligence technology has attracted much attention in recent years, and the progress of the technology is expected with the development of semiconductor technology. This talk focuses on synaptic mimic devices to realize artificial intelligence with semiconductor memory technology. These synaptic devices affect cognitive accuracy, along with conductance quantization and architecture. Therefore, we will first discuss from the architectural point of view and examine the characteristics of candidates for various synapse devices being reported. In particular, we concentrate on synaptic imitation devices that creatively use the functions of several flash memory devices. Finally, we discuss what features synaptic devices should have for neuromorphic applications, and how neuromorphic technology will evolve.

Jong-Ho Lee received the Ph.D. degrees from Seoul National University, Seoul, in 1993 in electronic engineering. In 1994, he was with the School of Electrical Engineering, Wonkwang University, Iksan, Chonpuk, Korea. In 2002, he moved to Kyungpook National University, Daegu Korea, as a Professor of the School of Electrical Engineering and Computer Science. Since September 2009, he has been a Professor in the School of Electrical and Computer Engineering, Seoul National University (SNU), Seoul Korea. He has been director of Inter-University Semiconductor Research Center (ISRC) at SNU since January 2018. From August 1998 to July 1999, he was with Massachusetts Institute of Technology, Cambridge, as a postdoctoral fellow. He has authored or coauthored 259 papers published in refereed journals and about 400 conference papers related to his research and has been granted 99 patents in this area. Prof. Lee is IEEE Fellow and a Lifetime Member of the Institute of Electronics Engineers of Korea (IEEE). He has been served as a subcommittee member of several international conferences including IEDM, ITRS ERD member, a general chair of IPFA2011, and IEEE EDS Korea chapter chair. He received 30 awards for excellent research papers and research excellence.
The tutorials will take place at the Auditorium Maximum of Jagiellonian University in Kraków on Monday, September 23, 2019

**Tutorial 1. Exhibition Room.**

**Nanoscale Technology, Transistor Modeling & IC Design**

**Chairs:** Wladek Grabiński (GMC, CH)  
Daniel Tomaszewski (ITE, PL)

**Abstract:**  
Our joint ESSDERC/ESSCIRC Tutorial aims to provide in-depth coverage of highly relevant R&D topics by world-class experts. We will discuss and present the frontiers of electron device modeling with emphasis on the complete UT SOI development chain, reviewing the nanoscale level technologies, devices TCAD numerical simulations, thru its simulation-aware compact/SPICE modeling up to selected topics of the transistor level IC design for advanced applications. This joint tutorial is designed for academic researchers, device process engineers who are interested in device modeling; academic/industrial ICs designers (to explore RF/Analog/Mixed-Signal) and those starting in these areas as well as device fabrication, electrical characterization, modeling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind the IC fabrication and its simulation in using modern SPICE/Verilog-A device models.

**Agenda:**

8:00 – 8:30 – Registration  
8:30 – 9:15 – [Technology: Guillaume Besnard, SOITEC (F) – UT SOI Processing and Device Fabrication](#) 
10:00 – 10:30 – Coffee break  
10:30 – 11:15 – [Devices: Thierry Poiroux, CEA-Leti (F) – Compact modeling for FDSOI technologies: Main challenges and possible solutions](#) 
11:15 – 12:00 – [Devices: Roberto Murphy, INAOE (MX) – RF Electrical Characterization](#) 
12:30 – 14:00 – [Lunch](#) 
14:00 – 14:45 – [Design: Christian Enz, EPFL (CH) – Systematic Design of Low-power Analog/RF CMOS Circuits using the Inversion Coefficient](#) 
15:30 – 16:00 – Coffee break  
16:00 – 17:00 – Panel discussion
Tutorial details

Speaker 1: Guillaume Besnard, SOITEC (F)
Title: UT SOI Processing and Device Fabrication
Abstract:
In this course, we will review the FDSOI manufacturing flow starting from SOI substrate fabrication up to the circuit ready for a test, alongside available options for device integration in sub-28nm technologies. We will also cover future challengers in processes, manufacturing tools and environment of advanced CMOS technologies. Finally, we’ll give a brief outlook of where the semiconductor industry is going based on current development trends.

Bio:
Guillaume Besnard joined SOITEC in 2012. Today, he belongs to R&D Collaboration Platforms group and is currently assigned at IMEC research center (Belgium), managing R&D programs in Logic, RF/Analog and Photonics. He received the Ph.D degree in Semiconductor Engineering from Institut National Polytechnique de Grenoble, France in 2016.

Speaker 2: Ahmed Nejim, Silvaco Inc. (USA)
Title: UT SOI TCAD Numerical Process/Device Simulation
Abstract:
Device and circuit design activities sit at the heart of technology development. Technology Computer Aided Design (TCAD) simulation is a powerful tool used to explore new process flows and device architectures. The ability to parametrise these simulations, allows users to effectively explore the available design space and optimise technology. Issues such as channel design, contact performance, transient behaviour and parasitic elements can all be captured in this activity. Furthermore, such simulation can be part of the development of SPICE models much needed for circuit and system design. SOI technology with ultra-thin buried oxide and fully depleted operation offers significant advantages for low power applications. However, issues such as parasitic elements as well as thermal effects are crucial considerations for the design activities. These coupled effects are inherently considered in the modelling of these devices in order to capture their full function. The talk will illustrate the numerical approach used in TCAD to showcase its value.

Bio:
Ahmed Nejim (male) obtained his PhD in 1990 in Ion-Solid interaction. A wide experience in ion implantation and semiconductor processing was obtained in 17 years of research in material science, semiconductor physics and microelectronic design. Experience in lecturing, mentoring and facility management. 10 years of technical project management, European multinational projects, Liaison research fellow of a UK national research facility in contact with national industry and national and international academia. Since 2001 he has been working at Silvaco supporting TCAD software users and developing collaborative projects. He acts as an R&D Project Manager for Silvaco Europe.
Speaker 3: Thierry Poiroux, CEA–Leti (F)
Title: Compact modeling for FDSOI technologies: Main challenges and possible solutions
Abstract:
Fully-Depleted Silicon-On-Insulator (FDSOI) technologies featuring Ultra-Thin silicon Body and Buried oxide (UT-SOI) have now entered into industrial production stage. These technologies present several decisive advantages over other options, such as excellent transistor electrostatic control, very low variability, simple planar process close to that of conventional bulk one, and very efficient back-bias effect. This latter feature allows a significant dynamic modulation of delay/power trade-off, which is a powerful know at circuit level. Therefore, to take full advantage of these technologies, circuit designer need compact models able to describe the transistor behavior over wide ranges of applied back biases, which actually requires considering FDSOI transistor as real Independent Double Gate (IDG) MOSFETs. In this tutorial, we will review the challenges that are to be addressed in order to build such compact models, from surface potential calculation to complete DC, AC and noise models.

Bio:
Thierry Poiroux received the M.S. degree from Ecole Centrale Paris, France, in 1995 and the Ph.D. degree from the University of Nantes, France, in 2000. His Ph.D. work was carried out at the Commissariat à l’Énergie Atomique/Laboratoire d’Electronique et de Technologie de l’Information (CEA–Leti), Grenoble, France, and Matra MHS on plasma process-induced damage. In 2000, he joined CEA–Leti as a Research Staff Member. Until 2002, he was involved in partially and fully depleted silicon-on-insulator (SOI) process integration and compact modeling. From 2002 to 2007, he worked on advanced device architectures and was in charge of multiple-gate device modeling and planar double gate process integration. In 2007, he started an activity on device integration on graphene, a promising material for the beyond complementary metal–oxide–semiconductor era. In 2011 and 2012, he has been the Head of the Innovative Device Laboratory of CEA–Leti. From 2012 to 2018, he worked on the development of the second version of Leti–UTSOI compact model, dedicated to fully-depleted SOI technology. Since 2018, he is the Head of the Simulation and Compact Model Laboratory of CEA–Leti. He has authored or co-authored five book chapters and more than 170 papers and communications, and he is author or co-author of about 20 patents.

Speaker 4: Roberto Murphy, INAOE (MX)
Title: RF Electrical Characterization
Abstract:
This talk will focus on the challenges involved in the characterization of MOS transistors in the high frequency regime, especially those related to calibration and de-embedding techniques. These aspects are of fundamental importance to define correct compact models for very high frequencies and smaller devices, as calibration standards deviate from ideal behavior, de-embedding techniques have to be based on more realistic structures, and user errors have to be minimized. Some guidelines to partially overcome these limitations are presented and discussed.
Bio:
Roberto S. Murphy-Arteaga received his B.Sc. degree in Physics from St. John’s University, Minnesota, and got his M.Sc. and Ph.D. degrees from the National Institute for Research on Astrophysics, Optics and Electronics (INAOE), in Tonantzintla, Puebla, México. He has been a researcher at INAOE since 1988. Since then, he has presented over 110 talks at scientific conferences, directed ten Ph.D., 18 M.Sc. and 2 B.Sc. theses, published more than 140 articles in scientific journals, conference proceedings and newspapers, and is the author of a text book on Electromagnetic Theory. He is currently a senior researcher with the Microelectronics Laboratory. Dr. Murphy’s research interests are the physics, modeling and characterization of the MOS Transistor and passive components for high-frequency applications, especially for CMOS wireless circuits, and antenna design. He is a Senior Member of IEEE, a Distinguished Lecturer of the Electron Devices Society, a member of the Mexican Academy of Sciences, and a member of the Mexican National System of Researchers (SNI).

Speaker 5: Christian Enz, EPFL (CH)
Title: Systematic Design of Low-power Analog/RF CMOS Circuits using the Inversion Coefficient
Abstract:
The emergence of the Internet of Things (IoT) poses stringent requirements on the energy consumption and has hence become the primary driver for low-power analog and RF circuit design. Implementation of increasingly complex functions under highly constrained power and area budgets, while circumventing the challenges posed by modern device technologies, makes analog and RF circuit design ever more challenging. Some guidance would therefore be invaluable for the designer to navigate the multi-variable design space. This tutorial presents low-power analog and RF design techniques that can be applied from device to circuit level. It starts with the presentation of the concept of inversion coefficient as an essential design parameter that spans the entire range of operating points from weak via moderate to strong inversion. Several figures-of-merit (FoM) including the and their product, capturing the various trade-offs encountered in analog and RF circuit design are presented. The simplicity of the base model is emphasized and compared against measurements of 40- and 28-nm bulk CMOS processes and BSIM6 simulations.

Bio:
Christian Enz, PhD, Swiss Federal Institute of Technology (EPFL), 1989. He is currently Professor at EPFL, Director of the Institute of Microengineering and head of the IC Lab. Until April 2013 he was VP at the Swiss Center for Electronics and Microtechnology (CSEM) in Neuchâtel, Switzerland where he was heading the Integrated and Wireless Systems Division. Prior to joining CSEM, he was Principal Senior Engineer at Conexant (formerly Rockwell Semiconductor Systems), Newport Beach, CA, where he was responsible for the modeling and characterization of MOS transistors for RF applications. His technical interests and expertise are in the field of ultralow-power analog and RF IC design, wireless sensor networks and semiconductor device modeling. Together with E. Vittoz and F. Krummenacher he is the developer of the EKV MOS transistor model. He is the author and co-author of more than 250
Speaker 6: Humberto Andrade da Fonseca (Cadence, US)

Title: Advanced SOI Design and Reliability/Ageing Simulations

Abstract:
In our talk we will present 28nm FDSOI and compare this process against conventional bulk technologies. We will then outline the design of a high-performance JESD receiver operating at 2.4Gbps with fast-tracking capability able to recover incoming data streams at over 5000ppm offsets. We will present a novel digital phase stepping method, taking advantage of a multi-phase ring oscillator, and the techniques to achieve ultra-low jitter in the PLL the key enablers for this performance. Besides the advantages of FDSOI other design aspects will be discussed with focus on mismatch, reliability analysis and aging considerations to address the durability requirements of the harsh automotive environment this design targeted. We will discuss the modular implementation used to easily scale the number of receiver lanes and how reliable and cheap at speed testing is enabled in production together with measurement results.

Bio:
Humberto Fonseca graduated with distinction in 2002 from the University of Porto. After a period at INESC researching FFT Algorithms, Fast Convolution, Spread Spectrum and DSP Architectures joined Chipdea Microelectronics’ PLL team, arising within it to the role of platform manager and taking the responsibility to develop and consolidate architectures for PLL and DLL based frequency and phase synthesisers for RF and High-Speed Wired Links. In 2007 after joining Texas Instruments took responsibility for the development of low jitter high-speed clocking components to support long reach SerDes at up to 25Gbps and later at Broadcom as Senior Principal lead the development of the Drivers and Reader front ends for the NFC family of controllers. In 2015 joined Cadence Design Systems to drive IP architecture in EMEA. Humberto has written a number of articles and holds several patents in NFC and clocking design.
Tutorial 2. Small Aula.
Circuits and Systems Enabling Quantum Technologies
Chair: Edoardo Charbon (EPFL Lausanne, CH)

Abstract:
Quantum technologies hold the promise to fundamentally change computing and other fields as we know them today. Most quantum technologies are based on quantum bits (qubits), which require to be constantly controlled, so as to ensure proper operation at deep-cryogenic temperatures. Electronic instruments operating at room temperature usually perform this control task, which also includes readout and evaluation. However, with the growth of qubit numbers, the complexity of these instruments is bound to increase exponentially, thus hindering the achievement of scalable quantum systems. Recently, a growing number of researchers has suggested moving the control electronics to cryogenic temperatures, to operate close to the qubits. In this tutorial, we capture this trend with nine speakers active in this field. We will discuss the latest developments of the field with a focus on cryogenic ICs leveraging over 60 years of technological advances in integrated electronics to ultimately achieve fully cryogenic systems for truly scalable quantum computers.

Agenda:
8:00 – 8:30 – Registration
8:30 – 9:15 – Jonathan Baugh (Univ. of Waterloo, CA) – Network architecture for a surface code quantum computer in silicon
9:15 – 10:00 – Tristan Meunier (CNRS Institut Néel, University Grenoble Alpe, FR) – Towards scalable silicon quantum computing
10:00 – 10:30 – Coffee break
10:30 – 11:20 – Christian Enz (EPFL, CH) – MOSFET Modeling down to Cryogenic Temperatures
11:20 – 12:10 – Philippe Galy (STMicroelectronics, FR) – FD-SOI CMOS technology towards silicon quantum applications with its cryogenic condition
12:10 – 13:00 – Alessandro Rossi (University of Strathclyde, Glasgow, UK & National Physical Laboratory, London, UK) – A dynamic random access architecture based on FD-SOI technology for radio-frequency readout of quantum devices
13:00 – 14:00 – Lunch
14:30 – 15:20 – Sorin Voinigescu (Univ. of Toronto, CA) – Towards monolithic quantum computing processors in production FD-SOI CMOS technology
15:30 – 16:00 – Coffee break
16:00 – 16:50 – Fabio Sebastiano (TU Delft, NL) – Cryogenic CMOS interfaces for large-scale quantum computers: from system and device models to circuits
16:50 – 17:40 – Joseph Bardin (Univ. of Massachusetts at Amherst, US) – CMOS Integrated Circuits for Control of Transmon Qubits
17:40 – 18:30 – Masoud Babaie (TU Delft, NL) – Benefits and Challenges of Designing Cryogenic CMOS RF Circuits for Quantum Computers
Tutorial details

Speaker 1: Jonathan Baugh, University of Waterloo, Waterloo, Canada
Title: Network architecture for a surface code quantum computer in silicon

Abstract:
Realizing a large-scale, universal quantum computer would enable major technological advances, yet presents a significant challenge. The standard circuit model for quantum computation requires a staggering error correction overhead to achieve fault tolerance. Topological stabilizer codes acting on two-dimensional qubit arrays, i.e. surface codes, can tolerate relatively high error thresholds and are very promising for scalability. I will present a brief introduction to quantum error correction, targeted to a non-quantum audience, to convey how fault tolerance is achieved in quantum computation. I will then describe our recent proposal for a network-of-nodes architecture that should allow practical scaling for a CMOS electron spin qubit processor.

Bio:
Jonathan Baugh is working toward the physical realization of quantum information processors in the solid-state, using the property of spin to encode and manipulate quantum information. Past work has focused on solid-state electron and nuclear magnetic resonance devices, and more recently on nanoelectronics devices including quantum wires and dots. Prior to joining the Institute for Quantum Computing at the University of Waterloo as a faculty member in 2007, he spent several years as a postdoctoral scholar and one year as a visiting researcher at the University of Tokyo. He received a PhD in Physics in 2001 from the University of North Carolina at Chapel Hill.

Speaker 2: Tristan Meunier, CNRS Institut Néel, University Grenoble Alpes, France
Title: Towards scalable silicon quantum computing

Abstract:
General considerations and recent achievements important to go to large-scale quantum computing in silicon will be discussed. The discussion will focus first on building deterministic and repeatable high quality, high fidelity qubit gates; second to demonstrate them within 2D arrays; and third to draw a projection on what a quantum computer based on Si would look like based on the learning of the two previous conditions. From a technological perspective, one main advantage of switching from lab to industry-like technology will be to provide access to advanced VLSI technology like 3D-integration to enable scaling of quantum systems in Si.

Bio:
Dr Tristan Meunier (CNRS Institut Néel, University Grenoble Alpes, France) is a CNRS researcher working at Institut Néel. His research interests are mainly in the field of coherent control of individual quantum objects, both in atomic physics and solid-state systems. Since 2005, he participates to the world-wide effort on the coherent control of individual electron spins in semiconductors. He received the Starting and Synergy Grants of the European Research Council (ERC) on the coherent control of individual electron spins in semiconductor nanostructures respectively in 2012 and 2018 (synergy together with Maud Vinet and Silvano DeFrancheschi).
Speaker 3: Christian Enz, EPFL, Lausanne, Switzerland
Title: MOSFET modeling down to cryogenic temperatures
Abstract:
There is currently a large effort to try to miniaturize quantum computers taking advantage of solid-state technologies enabling a potentially large number of qubits. CMOS is the preferred technology for building the qubit array and mixing it with the control and readout electronics taking advantage of the cryogenic temperature to operate the electronics at lower power and/or faster. The design and optimization of these CMOS analog and digital circuits need to have a compact transistor model that is valid down to cryogenic temperatures. Unfortunately, the MOSFET compact models available today do not scale properly with the temperature down to such low temperature. This presentation will address this limitation. It starts with an assessment of the analog performance at cryogenic temperatures using the simplified EKV MOSFET model. The main effects occurring at cryogenic temperature are described and a physics-based MOSFET model that scales down to ultra-low temperatures is presented.
Bio:
Christian Enz earned is PhD from EPFL in 1989. He is currently Professor at EPFL, Director of the Institute of Microengineering and head of the IC Lab. Until April 2013 he was VP at the Swiss Center for Electronics and Microtechnology (CSEM), where he was heading the Integrated and Wireless Systems Division. Prior to joining CSEM, he was Principal Senior Engineer at Conexant (formerly Rockwell Semiconductor Systems), Newport Beach, CA, where he was responsible for the modeling and characterization of MOS transistors for RF applications. His technical interests and expertise are in the field of ultralow-power analog and RF IC design and semiconductor device modeling. Together with E. Vittoz and F. Krummenacher he is the developer of the EKV MOS transistor model and the author of the book “Charge-Based MOS Transistor Modeling – The EKV Model for Low-Power and RF IC Design” (Wiley, 2006). He is the author and co-author of more than 260 scientific papers and has contributed to numerous conference presentations and advanced engineering courses. He is an IEEE Fellow and an individual member of the Swiss Academy of Engineering Sciences (SATW).

Speaker 4: Philippe Galy, STMicroelectronics, Crolles, France
Title: FD-SOI CMOS technology towards silicon quantum applications with its cryogenic condition
Abstract:
CQFD: It is well known that FD-SOI advanced CMOS technology is a good candidate for SOC integration and Low power applications. In this talk, we will give an overview of the 28nm FD-SOI technology with its key parameters and results. Afterward, we will discuss the quantum application and cryogenic temperature condition. Preliminary silicon results and innovative solutions in 28nm STMicroelectronics technology are introduced according to these challenges.
Bio: Philippe Galy was born in 1965; he received the Ph.D. from University of Bordeaux and H.D.R from LAAS CNRS University of Toulouse. He is a fellow and technical director at STMicroelectronics Research and Development France. He has proposed a full CDM protection and several new ESD compact devices for mature & advanced CMOS technologies. He supports several teams for research focused on new innovative solutions: Memory + silicon Qubit and cryo-design, Neuromorphic, 3D ultimate integration. He has authored or coauthored several publications (+100), books (3), and patents (+100). He serves in the TPC of and is a reviewer for many symposiums and journals. He is also involved in National (3) and European projects (3). Also he joins the QuEng CDP team from Grenoble

**Speaker 5: Alessandro Rossi, University of Strathclyde, Glasgow, UK & National Physical Laboratory, London, UK**

**Title:** A dynamic random access architecture based on FD-SOI technology for radio-frequency readout of quantum devices  

**Abstract:** Quantum computing is maturing at a relentless pace, yet individual quantum bits are wired one by one. As quantum processors become more complex, they will require efficient interfaces to deliver signals for control and readout while keeping the number of inputs manageable. Digital electronics could offer solutions to the scaling challenge by leveraging established industrial infrastructure to interface silicon-based quantum devices with conventional CMOS circuits. Here, we combine both technologies at millikelvin temperatures and demonstrate the building blocks of a dynamic random access architecture for efficient readout of complex quantum circuits. Our results demonstrate a path to reducing the number of input lines per qubit and enable addressing of large arrays of devices.

**Bio:** Alessandro is a Chancellor’s Fellow at Strathclyde University (Glasgow) and a Measurement Fellow at the National Physical Laboratory (London). His research interests span from quantum computing to quantum electrical metrology in semiconductor systems, as well as development of hybrid opto-electronic nanotechnology. Alessandro studied Electronic Engineering at the University of Naples (Italy) where he received his BSc and MSc summa cum laude. He was awarded a PhD in Physics by the University of Cambridge (UK). Alessandro has personally raised competitive early career grants and fellowships from British, European and Australian funding agencies. He was awarded Australia’s National Measurement Institute Prize in 2014, an EU’s Marie Curie Fellowship in 2015 and was elected a Junior Fellow at Cambridge University’s St Edmund’s College in 2016.

**Speaker 6: Sorin Voinescu, University of Toronto, Toronto, Canada.**

**Title:** Towards monolithic quantum computing processors in production FD-SOI CMOS technology  

**Abstract:** This presentation will discuss the feasibility of high-temperature (2-4 K) Si and SiGe electron/hole-spin qubits and qubit integrated circuits (ICs) in commercial 22nm FD-SOI CMOS technology and demonstrate the advantage
of the SiGe channel hole-spin qubit over its silicon-only electron-spin counterpart. It is also shown that, at 2 K, MOSFETs and cascodes can be operated as quantum dots in the subthreshold region, while behaving as classical MOSFETs and cascodes in the saturation region, suitable for qubits and mm-wave mixed-signal processing circuits, respectively.

Bio:
Sorin P. Voingescu holds the Stanley Ho Chair in Microelectronics and is the Director of the VLSI Research Group in the Electrical and Computer Engineering Department at the University of Toronto. He is an IEEE Fellow and a world-renowned expert on millimeter-wave and 100+Gb/s integrated circuits and atomic-scale semiconductor device technologies.

Speaker 7: Fabio Sebastiano, Delft University of Technology, Delft, Netherlands.
Title: Cryogenic CMOS interfaces for large-scale quantum computers: from system and device models to circuits
Abstract:
Quantum computers operate by processing information stored in quantum bits (qubits), which must typically operate at cryogenic temperature. A practical quantum computer will comprise thousands of qubits, thus requiring an electronic interface also operating at cryogenic temperature to ensure integration and scalability of the whole system. Focusing on the use of standard CMOS technology, we will explore the challenges in building such interface, comprising modeling of the quantum/classical interface, devices modeling for cryogenic CMOS and the design of high-performance cryogenic CMOS circuits. By demonstrating the cryogenic operation of complex CMOS analog and digital systems, we will show that cryogenic CMOS is a viable technology to enable large-scale quantum computing.

Bio:
Fabio Sebastiano holds degrees in Electrical Engineering from University of Pisa, Italy (BSc, 2003; MSc, 2005) from Sant’Anna School of Advanced Studies, Pisa, Italy (MSc, 2006) and from the Delft University of Technology, The Netherlands (PhD, 2011). From 2006 to 2013, he was with NXP Semiconductors Research in Eindhoven, The Netherlands. In 2013, he joined the Delft University of Technology, where he is currently an Assistant Professor. He has authored or co-authored one book, ten patents, and over 60 technical publications. His main research interests are cryogenic electronics for quantum applications, sensor read-outs and frequency references. Dr. Sebastiano was the co-recipient of the best student paper award at ISCAS in 2008, the best paper award at IWASI in 2017 and the best IP award at DATE in 2018. He is a senior member of IEEE, a TPC member for RFIC and a Distinguished Lecturer of the IEEE Solid-State Circuit Society.

Speaker 8: Joseph Bardin, University of Massachusetts, Amherst, U.S.A.
Title: CMOS Integrated Circuits for Control of Transmon Qubits
Abstract:
Future quantum computing systems will require cryogenic integrated circuits to control and measure millions of qubits. In this talk, we will first describe the unique challenges inherent to the control of superconducting qubits. Next, we will present the design and measurement of a prototype cryogenic
CMOS integrated circuit that has been optimized for the control of transmon qubits. The circuit has been integrated into a quantum measurement setup and its performance has been validated through multiple quantum control experiments. The talk will conclude with a discussion of challenges that must be overcome to enable scalable quantum computing.

Bio:
Joseph Bardin received the PhD in electrical engineering from California Institute of Technology in 2009. In 2010, he joined the Department of Electrical and Computer Engineering at the University of Massachusetts Amherst, where he is currently an Associate Professor. His research group pursues a wide range of topics related to integrated circuits for low-temperature applications, including radio astronomy, quantum optics, and quantum computing. Since the summer of 2017, he has also been with the Google Quantum AI group, where he has investigated the use of cryogenic integrated circuits for quantum computing. He has been the recipient of several awards including the DARPA YFA Award, the NSF CAREER Award, the ONR YIP Award, the UMass College of Engineering Outstanding Junior Faculty Award, and the UMass Award for Outstanding Accomplishments in Research and Creative Activities.

Speaker 9: Masoud Babaie, Delft University of Technology, Delft, Netherlands.
Title: Benefits and Challenges of Designing Cryogenic CMOS RF Circuits for Quantum Computers
Abstract:
Accurate and low-noise generation and amplification of microwave signals are required for the manipulation and readout of quantum bits (qubits). A fault-tolerant quantum computer operates at deep cryogenic temperatures (i.e. <100 mK) and requires thousands of qubits for running practical quantum algorithms. CMOS radio-frequency (RF) integrated circuits operating at cryogenic temperatures down to 4K (Cryo-CMOS) can offer a higher level of system integration and scalability for future quantum computers. In this presentation, I extensively discuss the role, benefits, and constraints of cryogenic CMOS RF circuits for control and readout of quantum bits. The main characteristics of the CMOS transistors and their impacts on RF circuit designs are described. Furthermore, opportunities and challenges of low-noise RF signal generation and amplification are investigated.

Bio:
Masoud Babaie received the Ph.D. degree (cum laude) in electrical engineering from the Delft University of Technology in 2016. In 2006, he joined the Kavoshcom Research and Development Group, Tehran, where he was involved in designing wireless communication systems. From 2009 to 2011, he was a CTO of that company. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined Delft as an Assistant Professor. His current research interests include RF/millimeter-wave integrated circuits and systems for wireless communications, and cryogenic electronics for quantum computation. Dr. Babaie has been a Committee Member of Student Research Preview (SRP) of the IEEE International Solid-State Circuits Conference (ISSCC),
since 2017. He was a recipient of the 2015–2016 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award.

**Tutorial 3. Main Auditorium B.**

**5G Radios: Concepts, Systems, and Silicon**

**Chairs:** Gernot Hubert (Silicon Austria Labs, AT)
Francois Rivet (IMS Bordeaux, FR)

**Abstract:**
The future of mobile communication specified in 5G includes sub-6 GHz frequency bands, mm-Wave frequencies (28 GHz, 39 GHz) for very high throughput in enhanced Mobile Broadband, Ultra-Reliable Low Latency Communications and Massive Machine Type Communication. This diversity, including their specific challenges demands from RFIC designers to discover innovative architectures and smart techniques to enable novel products. This workshop will provide the community in-depth understanding of new and underlying concepts and systems in 5G, including the advantages and challenges of Massive MIMO and beam-forming, as well as RFIC design examples such as 5G mm-Wave circuits for transceivers and key building blocks. The motivation of this workshop is to capture the lead-edge of IC design, what is the demand of the industry in the context of innovation in line with novel process technologies, as well, what are circuit and architectural concepts that are demanded. We focus especially on RFIC circuits design and technologies competing for today’s and tomorrow’s applications in 5G.

**Agenda:**
8:00 – 8:30 – Registration
8:30 – 9:00 – Introduction
9:00 – 10:00 – Fredrik Tillman (Ericsson, SE) – Going from a 5G Vision to Real Implementation
10:00 – 10:30 – Coffee break
10:30 – 11:30 – Marc Tiebout (Infineon, AT) – RFIC Design in BiCMOS for 5G mmWave Phased Arrays
11:30 – 12:30 – Ewout Martens (Imec, BE) – Advanced Techniques for ADCs for 5G Massive-MIMO
12:30 – 13:45 – Lunch
13:45 – 14:45 – Baudouin Martineau (CEA-LETI, FR) – Opportunity of CMOS FD-SOI for 5G
14:45 – 15:45 – Mirjana Videnovic-Misic (Silicon Austria Labs, AT) – Body Biasing in 28nm UTBB FD-SOI CMOS Technology – a Device Approach to enable 5G RFICs
15:45 – 16:15 – Coffee break
16:15 – 17:15 – Andrea Cathelin (STMicroelectronics, FR) – FD-SOI integration solutions for 5G Applications
17:15 – 18:00 – Gernot Hubert (Silicon Austria Labs, AT) – Very high data-rate RF Systems for beyond 5G
**Tutorial details**

**Speaker 1: Fredrik Tillman (Ericsson, SE)**  
**Title: Going from a 5G Vision to Real Implementation**

**Abstract:**  
Stretching beyond traditional mobile access, 5G is on a quest to transform connectivity as we know it today. With the ambition to provide data sharing anywhere at any time, for anyone and anything, the implementation challenges are demanding. This will also change the network deployment strategy and associated hardware realization in a profound way. On top, the spectrum availability has never been more diverse, which will further challenge traditional architectural approaches. This workshop presentation will highlight different 5G scenarios and their implications on the transceiver hardware. Transceiver block-level requirements will be discussed, as well as tradeoffs in terms of building practice, antenna integration, and cost.

**Bio:**  
Fredrik Tillman received his Msc and PhD in Circuit Design from Lund University in 2000 and 2005 respectively. From 2006 through 2007 he worked on CMOS RF ASIC design at Ericsson Mobile Platforms in Lund (Sweden) and Raleigh (USA). Since 2008 Dr. Tillman has been a technical manager at Ericsson Research with focus on CMOS circuit design, and acted as the Ericsson responsible for several European collaboration projects. In 2015 Dr. Tillman worked on the Ericsson radio DOT system in Ottawa (Canada) and is currently heading the Integrated Radio Systems department at Ericsson Research.

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**Speaker 2: Marc Tiebout (Infineon, AT)**  
**Title: RFIC Design in BiCMOS for 5G mmWave Phased Arrays**

**Abstract:**  
The infrastructure deployment of mm-Wave 5G telecommunications requires cost-effective, worldwide usable, easy to calibrate and long-term reliable RFICs. This talk will start with worldwide standardization requirements for infrastructure, next go into optimal technology choice, adequate system and RFIC partitioning, before introducing a BiCMOS RFIC chip set supporting worldwide 5G mmWave deployment. Last but not least the topic of integrated built-in test equipment supporting production testing and phased array calibration will be presented.

**Bio:**  
Marc Tiebout (S’90-M’93) was born in Asse, Belgium, in 1969. He received the M.Sc. degree in electrical and mechanical engineering in 1992 from the Katholieke Universiteit Leuven, Belgium, and the Ph.D. degree in electrical engineering from the Technical University of Berlin, Germany, in 2004. In 1993, he joined Siemens AG, Corporate Research and Development, Microelectronics in Munich, Germany, designing analog integrated circuits in CMOS and BiCMOS technologies. From 1999 to 2005, he was with Infineon Technologies AG, Munich, Germany, where he worked on RFCMOS circuits and transceivers for cellular wireless communication products and conducted highest frequency RFCMOS research for 17 and 24 GHz applications. Since 2006, he is with Infineon Technologies, Villach, Austria where his work includes Wimedium-UWB CMOS SoC development and mmWave phased-array
applications for radar, security and communications up to 80GHz. He has authored and co-authored more than 100 IEEE publications and more than 45 patents.

**Speaker 3: Ewout Martens (Imec, BE)**  
**Title: Advanced Techniques for ADCs for 5G Massive-MIMO**  
**Abstract:**  
Advanced Techniques for ADCs for 5G Receivers Abstract: In 5G systems, ADCs play a key role to increase the capacity and flexibility of the network. Depending on the system architecture, different scenarios result in different requirements for the ADCs. In handheld devices, the focus is on low power design solutions and high bandwidths with moderate accuracy. In baseband stations, recent advances in technology and design techniques enable low-power Giga-sampled ADCs supporting direct-RF architectures. For massive MIMO systems, low-power, low-area solutions are needed to realize digital-intensive architectures. To accommodate for different use cases, flexible ADCs with e.g. a variable resolution are preferred. Design cases of ADCs suitable for high-performant 5G systems will be discussed.  
**Bio:**  
Ewout Martens (M’08) was born in Genk, Belgium in 1978. He received the M.Sc. degree in 2001 and Ph.D. degree (summa cum laude) in 2007 from the Katholieke Universiteit Leuven, Belgium. From 2001 to 2007, he was a Research Assistant with ESAT-MICAS Laboratories of the Katholieke Universiteit Leuven. His Ph.D. research was on model-ing of Delta-Sigma modulators and RF front-ends. He joined imec (SSET), Belgium, in 2010 as a Design Engineer for WLAN transceivers. His interests and work are related to the development of innovative architectures for RF receiver front-ends, transceiver building blocks like PLL, filters and LNA, and ADCs for various applications including image sensors and wireless receivers.

**Speaker 4: Baudouin Martineau (CEA-LETI, FR)**  
**Title: Opportunity of CMOS FD-SOI for 5G**  
**Abstract:**  
CMOS circuits operating from analog to RF have proven their capability to satisfy the market demand in terms of cost and high volume capability. However, the upcoming RF to millimeter-wave products from IoT to 5G need improvements of performances and efficiency. This talk attempts to demonstrate that FD-SOI technologies are not only suitable for low power but also for high power RF circuit if proper design taking benefits of the technology is adopted.  
**Bio:**  
Baudouin Martineau received the Ph.D. degree in microwave and microtechnology in 2008. His Ph.D. thesis focused on the 65nm CMOS SOI potentialities for millimeter-wave wireless applications. In 2008, he joined the Technology R&D department of STMicroelectronics and now he is with CEA-LETI Research Institute as a senior research engineer in Analog-RF & mmW design activity.
Speaker 5: Mirjana Videnovic-Misic (Silicon Austria Labs, AT)
Title: Body Biasing in 28nm UTBB FD-SOI CMOS Technology – a Device Approach to enable 5G RFICs
Abstract:
As wireless networks are transitioning to 5G, there is a high demand for innovative wideband transceivers that will support the growing number of bands in an area and cost-efficient manner. Stringent system-level requirements, new application scenarios together with continuing downscaling and voltage supply decrease impose novel design methodologies and use of innovative semiconductor technologies like 28nm UTBB FD SOI CMOS. In this presentation, body biasing technique advantage given to a mixer-first receiver design will be explained from the device perspective. Area and circuit complexity reduction will be achieved for class A and class AB amplifiers while keeping tight control over important figures of merit in all process corners.
Bio:
Dr. Mirjana Videnović-Mišić received her PhD degree from the University of Novi Sad, Serbia, in 2009. From 2010 to 2016 she was an Assistant Professor at the Department of Electronics, Faculty of Technical Sciences, University of Novi Sad, Serbia. Dr. Videnović-Mišić was Fulbright Visiting Scholar at UC Berkeley from 09/2014-06/2015 and Marie Sklodowska Curie Fellow from 07/2015-06/2018. Her research interests include noise modeling of submicron components, design and optimization of analog and radio-frequency integrated circuits for the next-generation mobile devices. Dr. Videnović-Mišić joined Silicon Austria Labs in 2018.

Speaker 6: Andreia Cathelin (STMicroelectronics, FR)
Title: FD-SOI integration solutions for 5G Applications
Abstract:
This tutorial presentation will first present a very short overview of the major analog and RF/mmW technology features of the 28nm FDSOI technology. Then we will focus on the benefits in the view of 5G applications. Design examples such as a 30GHz 5G Power Amplifier, as well as an IoT Ultra Low Power SoC for WSN are given. A special focus will be done on the advantages of the unique features of body biasing in FD-SOI and specific design techniques offering state of the art performance.
Bio:
Andreia Cathelin (M’04, SM’11) started electrical engineering at the Polytechnic Institute of Bucharest, Romania and graduated from ISEN Lille, France in 1994. In 1998 and 2013 respectively, she received PhD and “habilitation à diriger des recherches” (French highest academic degree) from the Université de Lille 1, France. Since 1998, she has been with STMicroelectronics, Crolles, France, now Technology R&D Fellow. Her focus areas are in the design of advanced RF/mmW/THz and ultra-low-power circuits and systems.
Andreia has had numerous responsibilities inside IEEE since more than 15 years: at ISSCC, VLSI Symposium and ESSCIRC for TPC and Executive/Steering Committees respectively, and has been SSCS elected Adcom member 2015 to 2017. Andreia is a co-recipient of the ISSCC 2012 Jan Van Vessem Award and of the ISSCC 2013 Jack Kilby Award and the winner of the 2012 STM Technology Council Innovation Prize, for having introduced on the company’s roadmap the integrated CMOS THz technology for imaging applications. Andreia is ESSCIRC TPC Vice-Chair in Cracow 2019, and will be the TPC chair of ESSCIRC 2020 in Grenoble.
Tutorials

Tutorial 4. Medium Aula A.
Low-power RF and Analog Circuits

Chairs: Masoud Babaie (TU Delft, NL)
Teerachot Siriburanon (UCD Dublin, IE)

Abstract:
To support the exponential growth of the Internet of Things (IoT) devices, there has been significant development of research in ultra-low-power radios and low-power sensors aiming to improve efficiency and reduce cost. This tutorial consists of six talks by leading experts in a variety of key aspects of low-power analog and radio-frequency (RF) circuits design for IoT and healthcare applications, in particular, recent advancements in low-power analog and radio-frequency (RF) circuits design. This tutorial will include wireless communication and power links for micro-implantables, design of switch-capacitor DC-DC converters, low-power SAR ADCs, ultra-low-power receivers, energy-efficient digital transmitter design for IoT and healthcare applications, and ultra-low-power DTC-Based fractional-N digital PLL techniques.

Agenda:
8:00 – 8:30 – Registration
8:30 – 8:45 – Introduction
8:45 – 10:00 – Amin Arbabian (Stanford University, US) – Wireless Communication and Power Links for Micro-Implantables
10:00 – 10:30 – Coffee break
10:30 – 11:45 – Ravi Karadi, Gerard Villar Pique (NXP Semiconductors, NL) – Design of Switched-Capacitor DC-DC Converters
11:45 – 13:00 – Pieter Harpe (TU Eindhoven, NL) – Low-Power SAR ADCs
13:00 – 14:00 – Lunch
14:15 – 15:30 – Antonio Liscidini (University of Toronto, CA) – Ultra-Low-Power Receivers
15:30 – 16:00 – Coffee break
16:00 – 17:15 – Yao-Hong Liu (Imec, NL) – Energy-efficient digital transmitter design for ingestible (swallowable) applications
Tutorial details

Speaker 1: Amin Arbabian, Stanford University, USA
Title: Wireless Communication and Power Links for Micro-Implantables
Abstract:
Highly miniaturized minimally invasive implants with wireless power and communication links have the potential to enable closed-loop treatments and precise diagnostics. As with wireless power transfer, robust wireless communication between implants and external transceivers presents challenges and tradeoffs with miniaturization and increasing depth. Both link efficiency and available bandwidth need to be considered for communication capacity. This talk will overview various electromagnetic and ultrasonic communication and power links for implantable devices. We’ll review circuits and systems for robust bi-directional links and explore opportunities in achieving high-rate ultrasonic data communication with deep tissue implants using available spatial degrees of freedom.
Bio:
Amin Arbabian received his Ph.D. degree in EECS from UC Berkeley in 2011 and in 2012 joined Stanford University, as an Assistant Professor of Electrical Engineering. His current research interests include mm-wave and high-frequency circuits and systems, imaging technologies, Internet-of-Everything devices including wireless power delivery techniques, and medical implants. Prof. Arbabian currently serves on the steering committee of RFIC, the technical program committees of RFIC and ESSCIRC, and as associate editor of the IEEE Solid-State Circuits Letters (SSC-L) and the IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology (J-ERM). He is the recipient or co-recipient of the 2016 Stanford University Tau Beta Pi Award for Excellence in Undergraduate Teaching, 2015 NSF CAREER award, 2014 DARPA Young Faculty Award (YFA) including the Director’s Fellowship in 2016, 2013 Hellman faculty scholarship, and best paper awards from several conferences including ISSCC (2010), VLSI Circuits (2014), RFIC symposium (2008 and 2011, 2nd place), ICUWB (2013), PIERS (2015), MTT-S BioWireless symposium (2016), and BioCAS (2017).

Speaker 2: Ravi Karadi, Gerard Villar Pique, NXP Semiconductors, the Netherlands
Title: Design of Switched-Capacitor DC-DC Converters
Abstract:
Switched-capacitor DC-DC converters (SCPC) are an interesting option (in addition to the inductive converters) to realize power conversion needs, especially in the fully integrated applications with acceptable power efficiencies. They have the desirable features of using only capacitors and switches in the power stage (no inductors), and the power stage can be scaled easily to suit the load requirements. In this tutorial, we will cover the basic working principle, various SCPC topologies and the control techniques. We will start with the discussion of the basic workings of the SCPCs with some details of the various loss mechanisms. Depending on the input and output voltage ranges to be accommodated at the desired efficiency, certain voltage conversion ratio(s) need(s) to be implemented. This requires knowledge of the SCPC topologies: will present an overview of the various classical as well
as recently discovered SCPC topologies covering both two-clock-phase topologies and multiple-clock-phase topologies. Then we will present and compare different control techniques of the SCPCs. We will present some implementation examples to illustrate the design issues and trade-offs in SCPCs.

Bio:
Ravi Karadi received the M.Tech. degree in electrical engineering from the Indian Institute of Technology Delhi in New Delhi, India in 2006. He is currently a Principal Scientist in the field of power management in the with NXP Semiconductors in Eindhoven, the Netherlands. His main research interests include Switched-Mode Power Converters, (fully integrated) DC/DC converters, class-D audio amplifiers and analog circuit design.

Speaker 3: Pieter Harpe, TU Eindhoven, the Netherlands
Title: Low-Power SAR ADCs
Abstract:
With the development of Internet-of-Things, the demand for low-power radios and low-power sensors has been growing rapidly in the past decade. The Analog-to-Digital Converter (ADC) is one of the key building blocks in these systems to digitize information from the analog or RF domain to the digital domain. In this tutorial, an overview of low-power ADC architectures is given first, where the strong and weak points of each architecture are described, and limitations are investigated. Besides conventional architectures, several new developments like hybrid converters and noise-shaping SAR ADCs are introduced as well. After this overview, the talk will focus on low-power SAR ADCs, and the limits of power consumption, resolution, speed, and chip-area will be studied. Various concrete design examples from the literature will be discussed in more detail to show some of the latest techniques that enable very low-power ADCs with state-of-the-art performance.

Bio:
Pieter Harpe received the M.Sc. and Ph.D. degrees from the Eindhoven University of Technology, The Netherlands, in 2004 and 2010, respectively. In 2008, he started as a researcher at Holst Centre imec, The Netherlands. Since then, he has been working on ultra-low-power wireless transceivers, with the main focus on ADC research and design. In April 2011, he joined the Eindhoven University of Technology where he is currently an Associate Professor on low-power mixed-signal circuits. Dr. Harpe is a co-organizer of the yearly workshop on Advances in Analog Circuit Design (AACD) and analog subcommittee chair for the ESSCIRC conference. He also served as ISSCC ITPC member and IEEE SSCS Distinguished Lecturer and is the recipient of the ISSCC 2015 Distinguished Technical Paper Award.

Speaker 4: Antonio Liscidini, University of Toronto, Canada
Title: Ultra-Low-Power Receivers
Abstract:
This talk will start with a brief introduction of the requirements of a wireless receiver and an overview of the most common architectures and techniques tailored for ultra-low power applications. In the second part of this presentation, the concept of current/device reuse will be discussed, providing
Speaker 5: Yao-Hong Liu, imec-Netherlands, the Netherlands

Title: Energy-efficient digital transmitter design for ingestible (swallowable) applications

Abstract:
In this tutorial, several design challenges and state-of-the-art of wireless transceiver for ingestible applications (e.g., capsule endoscopy) will be provided. In such applications, digital polar transmitter architecture is favoured because of the low-voltage operation, excellent energy efficiency, and capability of extensive self-calibration, etc. On the other hand, the constrain on power consumption, link budget and volume of ingestible wireless systems is at least an order more stringent than those for wearable or IoT applications. Several new design approaches and low-power implementation of the digital polar transmitters, including digital PA and PLL, will be discussed. A design example of a sub-nJ/b OFDM digital polar transmitter for ingestible will also be included.

Bio:
Yao-Hong Liu received his Ph.D. degree from National Taiwan University, Taiwan, in 2009. He was with Terax, Via Telecom (now Intel), and Mobile Devices, Taiwan, from 2002 to 2010, working on Bluetooth, WiFi and cellular wireless SoC products. Since 2010, he joined imec, the Netherlands.
Hi current position is Principal Membership of Technical Staff, and he is leading the development of the ultra-low power (ULP) RFIC design. His research focuses are energy-efficient wireless transceivers and radar for IoT and healthcare applications. He currently serves as a technical program committee of IEEE ISSCC and RFIC symposium.

Speaker 6: Kenichi Okada, Tokyo Institute of Technology, Japan
Title: Ultra-Low-Power DTC-Based Fractional-N Digital PLL Techniques
Abstract:
In this presentation, some design techniques for fractional-N digital PLL will be introduced to improve both jitter and power consumption for low-power wireless applications. A highly-linear and low-power DTC and TDC will be presented as well as system-level optimization. An isolated constant-slope DTC realizes 10bit 0.1mW operation with a 26MHz reference clock, and sub-ps INL is achieved. The DTC-based AD-PLL achieves FoM of -246dB with 0.98mW power consumption and -56dB worst-case fractional spur. For further power saving, duty-cycled FLL, sub-sampling/sampling switching, charge-recycling DTC, and transformer-based DCO for impedance peaking will be also explained, which achieves 0.265mw power consumption with FoM of -237dB at 2.4GHz. Finally, a DPLL-based ADC and a BLE transceiver using DPLL will be introduced.

Bio:
Kenichi Okada received the B.E., M.E., and Ph.D. degrees from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively. He joined Tokyo Institute of Technology in 2003, and he is now Associate Professor. He has authored and co-authored more than 400 journal and conference papers. His current research interests include a millimeter-wave wireless transceiver, digital PLL, and ultra-low-power RF circuits. He has worked as a TPC member of ISSCC, VLSI Circuits, and ESSCIRC, and Guest editors and Associate Editor of JSSC.
Tutorial 5. Main Auditorium A.
Basics of Jitter and Phase Noise

Chair: Ali Sheikholesami (University of Toronto, CA)

Abstract:
Jitter and Phase Noise characterize the timing precision of clock and data signals in a variety of applications such as data converters, wireline, and wireless systems. The first talk in this tutorial provides the basic definitions of jitter and phase noise, their properties, and their relationship to each other.
This talk will form the foundation for the subsequent three talks. The second talk will discuss how jitter is converted to noise in data converters, thereby affecting the signal-to-noise ratio and the effective number of bits in an ADC. This talk will also show how, in wireline communications, jitter reduces the timing margin available for clock and data recovery (CDR) circuits and poses significant challenges to signal integrity as the data rates march towards 100Gb/s/lane and beyond. In the third talk, phase noise in oscillators will be discussed. After a theoretical analysis of the phase noise generation in oscillators, several topologies will be compared with some emphasis on harmonic CMOS oscillators. In particular, this talk will show the evolution through the different class of operation from class B to class F by highlighting the pros and cons of each topology. The final talk in this tutorial will discuss the impact of phase noise in wireless applications. After an overview of the mechanisms that set the most challenging phase noise requirement in wireless transceivers, such as reciprocal mixing and modulation of the local oscillator, the structure of a typical frequency synthesizer will be analyzed by highlighting the most critical sources of phase noise. This talk ends with an overview of the metrics which relate phase noise and power dissipation in the phase-locked loop.

Agenda:
8:00 – 8:30 – Registration
8:30 – 10:00 – Ali Sheikholesami (University of Toronto, CA) – Fundamental Concepts in Jitter and Phase Noise
10:00 – 10:30 – Coffee break
10:30 – 12:00 – Nicola Da Dalt (AMD, US) – Jitter in Wireline and Data Converter Applications
12:30 – 14:00 – Lunch
14:00 – 15:30 – Piero Andreani (Lund University, SE) – Phase Noise in Oscillators
15:30 – 16:00 – Coffee break
16:00 – 17:30 – Antonio Liscidini (University of Toronto, CA) – Phase Noise in Wireless Applications
Tutorial details

Speaker 1: Ali Sheikholeslami, University of Toronto, CA
Title: Fundamental Concepts in Jitter and Phase Noise
Abstract:
Jitter and Phase Noise characterize the timing precision of clock and data signals in a variety of applications such as data converters, wireline, and wireless systems. This talk provides basic definitions of various types of jitter and phase noise, how they manifest themselves in different applications, and how they all relate to each other. The aim of this talk is to provide an intuitive understanding of jitter and phase noise and to serve as a foundation for the next three talks in this tutorial.

Bio:
Ali Sheikholeslami received the B.Sc. degree from Shiraz University, Iran, in 1990 and the M.A.Sc. and Ph.D. degrees from the University of Toronto, Canada, in 1994 and 1999, respectively, all in electrical engineering. In 1999, he joined the Department of Electrical and Computer Engineering at the University of Toronto where he is currently Professor. He was on research sabbatical with Fujitsu Labs in 2005-2006, and with Analog Devices in 2012-2013. His research interests are in analog and digital integrated circuits, high-speed signaling, VLSI memory design, and CMOS annealing. He has coauthored over 70 journal and conference papers, 10 patents, and a graduate-level textbook entitled “Understanding Jitter and Phase Noise – A Circuits and Systems Perspective”, Cambridge University Press. He was a co-author of the CICC2017 Outstanding Student Paper Award. Dr. Sheikholeslami served on the Memory, Technology Directions, and Wireline Subcommittees of the ISSCC in 2001-2004, 2002-2005, and 2007-2013, respectively. He currently serves as the Education Chair for both ISSCC and the Solid-State Circuits Society (SSCS). He is a Distinguished Lecturer (DL) of the Society and oversees its DL and webinar programs. He is an Associate Editor for the Solid-State Circuits Magazine, in which he has a regular column entitled “Circuit Intuitions”. He was an Associate Editor for the IEEE TCAS-I for 2010-2012, and the program chair for the 2004 IEEE ISMVL. Dr. Sheikholeslami has received numerous teaching awards including the 2005-2006 Early Career Teaching Award and the 2010 Faculty Teaching Award, both from the Faculty of Applied Science and Engineering at the University of Toronto. He is a registered professional engineer in Ontario, Canada.

Speaker 2: Nicola Da Dalt, AMD, US
Title: Jitter in Wireline and Data Converter Applications
Abstract:
This talk will discuss the fundamental, first-order aspects of jitter in wireline and data converters applications. The wireline part will focus mainly on the operation of a classical Clock and Data Recovery unit and will analyze the concepts of Jitter Generation, Jitter Transfer and Jitter Tolerance. The data converter part will first describe the effect of jitter on DACs and how to calculate the resulting SNR. Subsequently, the effect of jitter on the basic operation of Nyquist ADCs, Sigma Delta ADCs, and the resulting performance degradation will be covered.
Bio:
Nicola Da Dalt received the M.S. degree from the University of Padova, Italy, in 1994 and the Ph.D. degree from RWTH Aachen, Germany, in 2007, both in electrical engineering, with distinction. From 1996 to 1998 he was with CSEL, Turin, Italy, as a concept engineer for architectures and synchronization of data transmission networks. From 1998 to 2015 he was with Infineon Technologies, Villach, Austria, as Lead Principal engineer for analog mixed-signal design, and manager of the Clock and Interface Systems group. From 2015 to 2018 he was with the Programmable Solution Group of Intel Corporation, San Jose, California, as Analog Engineering Manager for the development of high-speed serial interfaces for FPGA applications. Since 2018 he has been with AMD, Santa Clara, California as Silicon Design Engineering Director, focusing on high-speed wireline transceivers. Dr. Da Dalt served on the Wireline Subcommittee of the ISSCC from 2011 to 2015. He is the recipient of the 2010 IEEE Transactions on Circuits and Systems Guillemin-Cauer Best Paper Award for his pioneering work on digital bang-bang PLLs, and the recipient of the 2017 ISSCC Outstanding Forum Speaker Award. He is co-author of the book “Understanding Jitter and Phase Noise – A Circuits and Systems Perspective”, Cambridge University Press. He has co-authored over 30 journal and conference papers and 12 granted patents.

Speaker 3: Pietro Andreani, Lund University, SE
Title: Phase Noise in Oscillators
Abstract:
As one of the truly fundamental analog functions in any wireless/wireline application, the voltage-controlled oscillator keeps attracting a great deal of well-deserved attention. In this presentation, we will investigate the mechanisms of phase noise generation in harmonic oscillators, including some recently published general results, after which we will analyze both classical and emergent oscillator architectures, describing pros and cons for each. Various techniques to achieve a very wide oscillator tuning range, and their impact on phase noise, will be illustrated as well.

Bio:
Pietro Andreani received the M.S.E.E. degree from the University of Pisa, Italy, in 1988, and the Ph.D. degree from Lund University, Sweden, in 1999. Between 2001 and 2007 he was chair professor at the Center for Physical Electronics, Technical University of Denmark. From 2005 to 2014 he had a 20% position as analog/RF designer at Ericsson AB in Lund, Sweden. Since 2007, he has been associate professor at the dept. of Electrical and Information Technology (EIT), Lund University, working in analog/mixed-mode/RF IC design. He was also the head of the VINNOVA Center for System Design on Silicon, hosted by EIT (2014-2016). He has been a TPC member of ISSCC (2007-2012), is a TPC member of ESSCIRC (chair of the Frequency Generation committee since 2012, TPC chair in 2014) and RFIC, and an Associate Editor of JSSC. He was an IEEE SSCS Distinguished Lecturer in 2017-2018. He has authored numerous papers on oscillators and phase noise.
Speaker 4: Antonio Liscidini, University of Toronto  
Title: Phase Noise in Wireless Applications  
Abstract:  
This talk will discuss the impact of phase noise in wireless applications. After an overview of the mechanisms that set the most challenging phase noise requirement in wireless transceivers, such as reciprocal mixing and modulation of the local oscillator, the structure of a typical frequency synthesizer will be analyzed by highlighting the most critical sources of phase noise. The talk will end with an overview of the metrics which relate phase noise and power dissipation in phase locked loop.  
Bio:  
Antonio Liscidini was born in Tirano, Italy, in 1977. He received the Laurea (summa cum laude) and Ph.D. degrees in electrical engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006, respectively. He was a summer Intern with National Semiconductors, Santa Clara, CA, USA, in 2003, studying poly phase filters and CMOS low-noise amplifiers. From 2008 to 2012, he was an Assistant Professor with the University of Pavia and a Consultant with Marvell Semiconductors, Pavia, in the area of integrated circuit design. In 2012, he moved to the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, where he is currently an Associate professor. His research interests are focused on analog mixed signal interfaces with particular emphasis on the implementations of wireless transceivers and frequency synthesizers for cellular and ultra-low power applications. Dr. Liscidini was a recipient of the Best Student Paper Award at the IEEE 2005 Symposium on VLSI Circuits and a co-recipient of the Best Invited Paper Award at the 2011 IEEE Custom Integrated Circuit Conference. He has served as an Associate Editor for the IEEE Transactions on Circuits and Systems II: Express Briefs (2008-2011) (2017-2018) and as a Guest Editor for the IEEE Journal of Solid-State Circuits (2013) (2016) and Guest Editor of the IEEE RFIC Virtual Journal (2018). Between 2016 and 2018, he has been a Distinguished Lecturer of the IEEE Solid-State Circuits Society. He has been member of the International Solid-State Circuit TPC (2012-2017), member of the European Solid-State Circuit Conference TPC (2010-currently) and member of the Custom Integrated Circuit Conference TPC (2019-currently).
Abstract:
The tutorial session aims to address the subjects related to the development of new THz detectors, amplifiers and sources in view of their application to passive and active imaging, security screening as well as to wireless communication systems. It is expected to demonstrate how new physical phenomena, new advances in materials technology as well as innovative devices design may lead to the development of new high-performance THz systems. Special accent will be put to THz properties of Graphene and graphene-like topological phases of semiconductor heterostructures of III-V or II-VI materials- like HgCdTe or quantum wells for example. Independently the tutorial has as an objective to make a review of recent developments of THz components and systems based on traditional semiconductor technology. The questions of the choice of the best semiconductor technology for THz imaging and wireless communications will be addressed. The speakers will be invited to present the problems of THz technology market and the problem of so-called “killer” application. Particular attention will be devoted to the realization of sensors for focal plane arrays for real-time imaging. The feasibility of the THz active and passive vision systems will be discussed. Summarizing the objectives of this Symposium are to review the current state of the art in THz components and systems in USA, Asia and Europe, to provide a clear view on the current technologies and the required advances in material science and devices to achieve more efficient systems.

Agenda:
Registration (starts from 8:00)
10:00 – 10:30 – Coffee break
13:00 – 14:00 – Lunch
14:00 – 14:45 – Michael Shur (Rensselaer Polytechnic Institute – Troy NY USA) – Terahertz Radiation Detection, Manipulation, and Emission using Plasma Oscillations in Field Effect Transistor Channels
14:45 – 15:00 – Sergey Ganichev (Regensburg THz center , TerZ and CENTERA) – Opto-electronic effects of THz radiation and their application on topological materials
15:30 – 16:00 – Coffee break
16:00 – 16:45 – Alydas Lisauskas (Vilnius University and CENTERA) – Terahertz integrated circuits for free-space applications
16:45 – 17:30 – Dmitri Lioubczenko (Royal Institute of Technology – Sweden and CENTERA) – Passive and active devices based on dielectric rod waveguides for millimeter and THz frequencies
17:30 – 18:15 – Wojciech Knap (IHPP-PAS Warsaw and L2C University of Montpellier&CNRS) – Transistors based THz detectors – from basic physics to first real-world applications
Tutorials

Tutorial details

Speaker 1: Michael Shur (Rensselaer Polytechnic Institute – Troy NY USA)
Title: Terahertz Radiation Detection, Manipulation, and Emission using Plasma Oscillations in Field Effect Transistor Channels
Abstract:
This tutorial will address the counter-intuitive physics of the ballistic transport in short channel semiconductor devices. It will focus on the plasma waves, which are the oscillations of the electron (or hole) density in a transistor channel. The equations describing the plasma oscillations are the hydrodynamic equations and the phenomena linked to the wave excitation and propagation in liquids all have their counterparts in the electronic or hole two-dimensional fluid. The nonlinearity of the electron transport leads to the rectification, frequency multiplication, or emission of the plasma waves with the commensurate detection or emission of sub-terahertz (sub-THz) or THz radiation. Transistors, heterostructures, nanostructure arrays, and metamaterials made of Si, GaAs, InGaAs, GaN, graphene, carbon nanotubes, and diamond all compete for the THz plasmonic applications. I will discuss the Dyakonov-Shur and “plasmonic boom” mechanisms of the plasmonic instabilities in the electronic fluid and will describe the emerging novel device designs, such as using “plasmonic stubs” to control the boundary and interface conditions. I will explain how the new regimes of the device operation, unique for the plasmonic transistors, enable the THz spectroscopy and interferometry. I will also present a new compact THz Field Effect Transistor model (implemented in SPICE and ADS). This model agrees well with the experimental data and is suitable for the design, parameter extraction, and characterization of the plasmonic transistors and circuits.
Bio:
Dr. Michael Shur is Roberts Professor at RPI and co-founder of Sensor Electronics Technology, Inc., and of Electronics of the Future, Inc. He has over 400 patents or patent applications and is Life Fellow of IEEE APS, ECS, and SPIE and Fellow of the National Academy of Inventors and of several other professional societies. His awards include IEEE Ebers, Kirchmayer, Donald Fink, and Sensors Council Awards, Tibbetts Award for Technology Commercialization, St. Petersburg Technical University and University of Vilnius Honorary Doctorates, Gold Medal of Russian Education Ministry, van der Ziel Award, Senior Humboldt Research Award, RPI Research Awards, and several Best Paper Awards. He is an IEEE EDS and Sensors Council Distinguished Lecturer and Foreign Member of the Lithuanian Academy of Sciences.

Speaker 2: Sergey Ganichev (Regensburg THz Center, TerZ and CENTERA)
Title: Opto-electronic effects of THz radiation and their application on topological materials
Abstract:
The paper overviews experimental and theoretical studies of photogalvanic and photon drag effects induced in various in three-dimensional (3D) and 2D topological insulators (TI) by polarized terahertz (THz) radiation. Photocurrent spectroscopy has been proven to be an important tool to study low-dimensional semiconductors graphene. In the last several years, it has been
If of frequencis of transistor. These include established results. Several physical mechanisms of Terahertz integrated circuits for free-space applications demonstrated that photogalvanics, magneto-photogalvanics and photon drag effect can also be efficiently used for probing topological surface and edge states. It is shown that THz radiation results in dc electric current, which is sensitive to the radiation polarization and may have a component changing the sign by reversing the radiation helicity. Photogalvanic and photon drag effects are very general and have already been demonstrated for different topological systems, including Bi$_1$-xSbxTe 3D TIs, HgTe-based 2D and 3D TIs, and Pb1-xSnxSe TIs with large value of x. A further tool to study TI states yields magneto-photogalvanic effects, particularly the cyclotron resonance assisted current observed in HgTe-based Dirac fermions systems.

Here we present the state-of-the-art of the field, including both recent advances and well-established results. Several physical mechanisms of photogalvanics in TI systems are described. We discuss the phenomenological and microscopic theory of these phenomena and present experimental achievements. We also show that nonlinear transport opens up new opportunities for probing of Dirac electrons as well as address prospective of future theoretical and experimental studies.

Bio:
Prof. Dr. Sergey Ganichev received the Diploma of Physics degree and the Ph.D. degree from the St. Petersburg Polytechnic University, Russia in 1980 and 1984, respectively. In 1997 he obtained the Dr. habil. degree from the Ioffe Physicotechnical Institute, St. Petersburg, Russia and in 2002 from the University of Regensburg, Germany. From 1980 till 2005 Prof. Dr. Ganichev has been working at the Ioffe Institute, St. Petersburg, Russia. In 1992 he joined the Institute for Experimental and Applied Physics at the University of Regensburg, Germany, where he is currently working as a full professor. His research interests are terahertz science and technology, nonequilibrium and nonlinear effects in semiconductors, tunneling and photoelectrical phenomena in semiconductors and semiconductor nanostructures, electron gas heating, Bloch oscillations, spin physics in semiconductors, physics of graphene and topological insulators, and ratchet phenomena.

Speaker 3: Alvydas Lisauskas (Vilnius University and CENTERA)
Title: Terahertz integrated circuits for free-space applications
Abstract:
This tutorial will present a survey on recent developments in the rapidly expanding field of integrated-circuit-based terahertz technologies. In addition to a standard approach in which active devices directly amplify THz frequencies, a large number of novel devices rely on nonlinear properties that manifest above the cut-off frequencies of transistors. These include multiplier-based THz sources, detectors, heterodyne and subharmonic mixers. For example, at low frequencies a field effect transistor-based rectifier rely on standard resistive mixing, however with rising frequency, charge-density waves (or plasma oscillations) in the channel start playing an increasingly important role and enable detection and mixing far beyond classical cut-off frequencies. An aspect whose significance cannot be overestimated is that efficient devices can be fabricated conveniently by Si CMOS foundry technologies. Examples of efficient implementation of THz detectors and detector arrays as well as THz sources for free-space coupling applications using standard integrated circuit fabrication techniques will be discussed.
Bio:
Dr Alyudas Lisauskas (male) – graduated from Physics Faculty of the Vilnius University and received PhD in 2001 at Royal Institute of Technology, Stockholm, Sweden. From 2002 till 2017 worked at Physikalisches Institut, Frankfurt University, Frankfurt am Main, Germany, since 2013 also in Vilnius University (since 2017 running the joint lab with CPST, Vilnius). Has extensive experience in techniques of THz generation, mixing and detection, including technologies for manufacturing relevant components. Published 109 papers that accumulated 1416 citations (h-index = 19). Won a competition for a team leader position in CENTERA WG3 and will be developing THz-related integrated circuits there.

Speaker 4: Dmitri Lyubchenko (Royal Institute of Technology – Sweden and CENTERA )
Title: Passive and active devices based on dielectric rod waveguides for millimeter and THz frequencies
Abstract:
The research and development in the frequency region of 0.1-1.5 THz is extremely significant for a wide range of applications, In spite of the problems in technology and high prices for basic components (e.g. phase shifters, directional couplers, etc.) in the THz systems meet expanding interest of consumers. Dielectric rod waveguides (DRW) are the promising transmission lines, when low loss dielectric materials are used and can be combined with semiconductor devices (oscillators, detectors, mixers, etc.) in the hybrid and/or monolithic integrated circuits. DRW offer a new opportunity for passive and active component performance, as it allows to decrease the insertion loss. Besides, DRWs have no cut-off frequency enabling broad band operation. In, the DRW antenna was proved to operate in the frequency band of 0.1-1.1 THz. The DRW is an open, i.e., not metal-shielded, waveguide system allowing to affect it with outside electro-magnetic fields including light. If one of the DRW walls is covered with a variable impedance layer, the propagation constant can be tuned. Existing materials with tunable electrical parameters are usually very lossy at upper millimeter-wave to THz frequencies. Thin layers of optically-controlled carbon nanotubes (CNTs) are proposed in this paper as a novel solution. The simplicity of the CNT deposition gives an opportunity to cover a large area, which is essentially important for e.g. for reflector surface coating, sensor matrices, etc. CNT compo-nents can be integrated with DRW antenna elements for THz beam steering applications.

Bio:
Dr Dmitri V. Lyubtchenko (male) – graduated from Moscow Institute of Physics and Technology and obtained PhD in 1997 at Institute of Radioengineering and Electronics, Russian Academy of Sciences, Moscow. Subsequently a postdoc at the University of Liverpool, UK. From 1999 worked at Helsinki University of Technology on the dielectric rod waveguides and passive and active devices for millimeter-wave integrated circuits based on these waveguides. In 2013-2017 senior scientist at Aalto University School of Science and Technology and since 2016 a Visiting researcher at Royal Institute of Technology, Stockholm. Published 70 papers, accumulating 519 citations.
Tutorials (h-index=10). Won a competition for a team leader position in CENTERA WG4 and will developing THz passive elements.

Speaker 5: Wojciech Knap (IHPP-PAS Warsaw and L2C University of Montpellier&CNRs)
Title: Nanotransistors based THz detectors – from basic physics to first real-world imaging applications

Abstract:
This talk will start with a brief introduction presenting different kinds of transistors that can be used for THz detection FETs (si-CMOS, HEMTs, and HBTs). Physical mechanisms responsible for THz radiation rectification will be discussed. The maximum theoretical responsivity of these different transistors will be compared. The theoretical introduction will be followed with examples of experimental studies of single transistors as well as their arrays. The postal security scanner will be presented as the main example of the THz scanner security application. Special attention will be paid to polarization-sensitive detection. We will show how the measurement of the radiation polarization can bring additional information in the nondestructive testing of different fiber injected materials.

Bio:
Prof. dr Wojciech Knap obtained his master and PhD degrees from Faculty of Physics – Warsaw University Poland. His PhD concerned the Terahertz (Far infrared) properties of narrow gap semiconductors HgTe and InSb. After his PhD degree (1985) he obtained a permanent assistant professor position at University of Warsaw Solid State Physics Department. In 1987 he left to France and worked at University of Montpellier, Grenoble High Magnetic Field Laboratory, Toulouse Pulsed High Magnetic Field Laboratory. In 1992 he obtained a permanent position at French National Centre for Scientific Research – CNRS – Montpellier. He worked as associated professor at USA – Rensellear Polytechnic Institute and Tohoku University Japan. His main scientific interests and activities are concentrated around Fair Infrared-FIR (Terahertz – THz) properties of semiconductors and in particular in basic physics and applications of Terahertz Plasma excitations in nanotransistors. He is currently coordinating/animating an International Laboratory – LIA-TERAMIR composed with 9 groups from France, Poland and Russia and CENTERA – EU founded Laboratory of THz science and technology in Warsaw.
Tutorial 7. Medium Aula B.
Technologies and Devices for IoT

Chair: Adrian Ionescu (EPFL, CH)

Abstract:
In the future, major innovations will require holistic approaches encompassing silicon and cloud technologies in the context of big/abundant data analytics. There is still a very important role to be played by innovations in energy efficient technologies, devices, and system architectures and design, building on the success of silicon CMOS. This tutorial is addressing some of the stringent challenges of Internet of Things and Edge Computing in terms of energy efficient technologies, sensor network architectures, energy harvesting, power management and the design in most advanced low power CMOS technologies such as Ultra-Thin Body Fully Depleted Silicon On Insulator. The speakers will detail the state of the art in the field and will illustrate their talks with concrete examples and implementations. A particular attention will be dedicated to the use of IoT in medicine and smart living.

Agenda:
8.00-8.30 - Registration
8:30 – 9:15 - Adrian Ionescu, EPFL, Switzerland – Energy efficient technologies and devices for enabling Artificial Intelligence at the Edge: an Overview
9:15 -10:00 - Emilio Calvanese Strinati, CEA-LETI, France – Smart IoT sensors for medicine and smart living
10:00-10.30 - Coffee break
10:30 – 11:15 - Thomas Skotnicki, CEZAMAT WUT, Poland & CENTERA Laboratories, UNIPRESS, Poland – Energy harvesting and power management for sub-milliWatt IoT nodes (I)
11:15 -12:00 - Mathieu Costans, EM Microelectronic, Marin, Switzerland and Maher Kayal, EPFL, Switzerland - Energy harvesting and power management for sub-milliWatt IoT (II)
12:00 – 12:45 - Stephane Monfray, ST Microelectronics, France – Designing ultralow power IoT systems with UTBB FD-SOI
12:45 – 13.00 - Q & A session with all speakers
13.00-14.00 - Lunch

Tutorial details

Speaker 1: Adrian M. Ionescu (EPFL, Switzerland)
Title: Energy efficient technologies and devices for enabling Artificial Intelligence at the Edge: an Overview
Abstract:
Analysts predict that by 2025 AI-related semiconductors will account for 20% percent of all semiconductor demand, corresponding to a $67 billion in revenue, at a growth rate that is 5x higher than the one in conventional semiconductor applications. This overview includes major trends in basic
hardware technologies needed to support the Artificial Intelligence Applications at the Edge: energy efficient sensing, computation and communications. We will illustrate some of the most promising trends in wearable computing and sensing. We will also highlight the importance of more decentralized strategies in AI, as the new breathing of the computer industry, with edge computing is a natural next step.

Bio:
Adrian M. Ionescu is a Professor at Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland. He is an IEEE Fellow and he served in the past for 2 terms (total of 6 years) as Editor of IEEE Transactions on Electron Devices and as a member. He received the B.S. &M.S. in Electronics and Telecommunications in 1989 from the University ‘Politehnica’ Bucharest, Romania. He holds two PhDs: in Microelectronics, from University ‘Politehnica’ Bucharest (1994) and in Physics of semiconductor devices from the National Polytechnic Institute of Grenoble, France (1997). He held staff and/or visiting positions at LETI-Commissariat à l’Énergie Atomique, Centre National de la Recherche Scientifique (CNRS), and Stanford University, USA, in 1998 and 1999. He was Invited Professor with Tokyo Institute of Technology, Japan, in 2012 and 2016.

Prof. Ionescu has published more than 500 articles in international journals and conference proceedings. He is the recipient of IBM Faculty Award 2013 for contributions to the Engineering of the André Blondel Medal 2009 of the Society of Electrical and Electronics Engineering, Paris, France. In 2015 he was elected as a member of the Swiss Academy of Sciences (SATW). In the same year, he received the Outstanding Achievement Award of SATW for the successful coordination and delivery of the first Swiss Technology Outlook. In 2016 he received the prestigious Advanced ERC (European Research Council) Grant for individual senior scientists in Europe to develop a 5-year research programs aiming at 100 millivolt switches and sensors for Internet-of-Things.

Speaker 2: Emilio Calvanese Strinati (CEA-LETI, France)
Title: Smart IoT sensors for medicine and smart living
Bio:
Emilio Calvanese Strinati obtained his Engineering Masters degree in 2001 from the University of Rome ‘La Sapienza’ and his Ph.D in Engineering Science in 2005 on Radio link control for improving the QoS of wireless packet transmission. He then started working at Motorola Labs in Paris in 2002. Then in 2006 he joint CEA/LETI as a research engineer. From 2007, he becomes a PhD supervisor. Since 2011 he is the Smart Devices & Telecommunications European collaborative strategic programs Director. E. Calvanese Strinati has published around 70 papers in international conferences and books chapters, and is the main inventor or co-inventor of more than 50 patents. He has organized more than 30 international workshops and special sessions on green communications and heterogeneous networks hosted in international conferences as IEEE GLOBECOM, IEEE PIMRC, IEEE WCNC, IFIP, and European Wireless. Dr. Calvanese Strinati has been the co-chair of the wireless working group in GreenTouch from April 2010 to January 2012. Since 2012 he is the strategy director of the Smart Devices & Telecommunications Strategy Program Director and in 2013 he has been elected as one of the 5G PPP steering board members.
Speaker 3: Thomas Skotnicki (CEZAMAT WUT, Poland & CENTERA Laboratories, UNIPRESS, Poland)

Title: Energy harvesting and power management for sub-milliWatt IoT nodes (I)

Abstract:
Internet of Things involves a huge number of communicating devices deployed in our environment as well as in surrounding objects. Related to IoT terms such as: Smart Planet, WSN (wireless sensor nets), Swarm, TSensors (trillion sensors), Internet of Everything, M2M (machine to machine), Smart Dust, etc. give an idea of the global and ubiquitous dimension of IoT. The economical aspect of IoT is also hard to be overestimated since none of the former High Tech revolutions has reached the volume of trillion unit market. This new enormous dimension of the market sets many new technical challenges, and among them the question of powering the IoT devices. The usage of batteries for this purpose could seem the simplest and the most natural, if not the fact that IoT devices will be often placed in inaccessible loci (in the volume or elements of constructions, buildings, machines, cars, industrial installations, urban infrastructure, rural vast areas, etc.). Changing trillions of batteries periodically may thus turn out to be more difficult and costly than their fabrication and deployment. Therefore, energy self-sustainability or self-powering of IoT devices is considered a key feature. In this SC we will deliberate on main kinds of energy harvesters (PV, TEGs, vibrational, EM and RF). We will explain their operation principles, pros and cons, their state of the art, and their development perspectives and challenges.

Bio: Thomas Skotnicki was with France Telecom from 1985 till 1999 when he joint STMicroelectronics. He became the first STMicroelectronics Company Fellow and Technical Vice-President. He invented the UTBB FDSOI structure (in production at STMicroelectronics, GF and Samsung). Today he is the Co-Leader of the CENTERA project (International Research Agenda funded by Foundation for Polish Science), Director of the CEZAMAT Consortium and Professor at Warsaw University of Technology, Poland. He holds 80 patents and has authored close to 400 scientific papers, and several book chapters on CMOS and Energy Harvesting. His models/software MASTAR were used by ITRS for 12 consecutive editions for calculations of CMOS roadmaps. He is an IEEE Fellow, has supervised 31 PhD theses, during 8 years served as Editor for IEEE TED, was on JJ Ebers and Frederik Philips IEEE Award Committees, and served in Executive Committees of all big conferences in his field (IEDM, Symposia on VLSI, ESSDERC, ICSICT, ECS, etc).
Speaker 4: Mathieu Coustans (EM Microelectronic, Marin, Switzerland), Maher Kayal (EPFL, Switzerland)
Title: Energy harvesting and power management for sub-milliWatt IoT (II)
Abstract:
Computing at the edge, in the fog, or in the cloud is Building on the success of scaling of silicon CMOS. Nowadays mm³ computing defines the state of the art in terms of integration including the whole functions needed to operate an edge node in the sub-milliWatt region. Such computers are comparable to a grain of sea salt. In this context, there is still a very important role to be played by innovations in energy efficient technologies, devices, design, and system architectures. This tutorial paper is addressing some of the stringent challenges of Internet of Things and Edge Computing in terms of energy efficient technologies. It attempt at providing some scaling number based estimation of the power load and a focus on power management and energy harvesting circuits in CMOS technologies.

Bio:
Mathieu Coustans received the M.S. degree in Electrical Engineering from ENSEEIHT Toulouse in 2014 and Ph.D Degree from the Ecole Polytechnique Fédérale de Lausanne (EPFL) in 2019. He was mixed signal designer for Thales Alenia Space from 2011-2014. He joined EM Microelectronic, Marin, Switzerland during the first Quarter of 2015. From March 2015 to December 2018 he was working towards the Ph.D degree at the Electronics Laboratory at the EPFL. His work focused on ultra-low power design methodology for frequency generation in the IoT design space. He Joined EM Microelectronic, Marin, From January 2019 until April 2019 as a Senior mixed-signal designer in the Emerging Business, Business-unit. He has published a dozen scientific papers, co-authored text books dedicated to power-management in the internet of everything, and holds three patents.

Bio:
Maher Kayal received the M.S. and Ph.D degrees in electrical engineering from the Swiss Federal Institute of Technology Lausanne (EPFL), Lausanne, Switzerland in 1983 and 1989, respectively. He has been with the Electronics Laboratories, EPFL, since 1990, where he is currently a Professor and the Director of the Energy Management and Sustainability section. He has authored many scientific papers, co-authored five text books dedicated to mixed-mode CMOS design and he holds nine patents. His current research interests include analog and mixed-signal circuits design including highly linear and tunable sensors microsystems, signal processing, and green energy management. Mr. Kayal was a recipient of the Swiss Ascom Award in 1990 for the best work in telecommunication fields, several awards in the ED and TC Conference in 1997, the IEEE-AQTR in 2006, the Mixdes Conference in 2009, and the Power Tech Conference in 2009, the Poland Section IEEE ED Chapter Special Award in 2011, the Swiss Credit Award for best teaching in 2009, and the Electronics Letters Journal Premium Award in 2013.
Speaker 5: Stephane Monfray (ST Microelectronics, France)
Title: Designing ultralow power IoT systems with UTBB FD-SOI

Abstract:
As IoT market is booming, the role of energy harvesting will be a key enabler for the development of abandoned sensors. Thanks to the conjunction of ultra-low power electronic development and by changing the paradigm of energy harvesting, the integration of autonomous sensors and electronics with ambient energy harvesting will be achievable. The tutorial will address innovative solutions for implementing optimized systems to demonstrate complete ultra-low power autonomous wireless sensors working with μW power, and we will focus on solutions offered by CMOS compatible technologies: FDSOI low power circuits, innovative power management to optimize energy harvesting, and what silicon technologies can provide for innovative energy harvesters.

Bio:
Dr. Stéphane Monfray is the Principal Scientist in the Silicon Technologies Department at STMicroelectronics in Crolles (ST SAS C2). He is born 1975, obtained his Ph.D. from the University of Provence (France) in 2003 and owns an engineering degree in Semiconductor Science from INSA Lyon (National Institute of Applied Sciences). Since 2008, he is a member of the STMicroelectronics Experts staff. He was involved in FP6 and FP7 projects (Nanocmos, Pullnano, Duallogic, COMPOSE3), H2020 (NEIRED, COSMICC) and led from 2012 to 2016 a national project (FUI) on energy harvesting. He is the author and co-author of more than 125 publications in major conferences and journals, of more than 50 patents, of a book chapter. He had multiple participations and paper presentations at conferences and contributes now with several invited talks every year. His experiences and expertise are on advanced CMOS, Energy Harvesting and IoT systems, and advanced active Photonic devices. His activities are now focused on the development of advanced technologies for Sensors and Photonic devices for automotive (gyroscopes, sensors, LiDAR). He was the co-recipient of the Paul Rappaport Award in 2000, and he is the co-recipient of the 2012 French Electronic Grand Prize “General Ferrié” for his work on thin-film devices.
The Workshop will take place at the Auditorium Maximum of Jagiellonian University on Monday, September 23, 2019.

Workshop. Seminar Room.

Heterogeneous Integration of Nanomaterials and Innovative Devices

Organizer: SiNANO Institute

Abstract:
The SiNANO Institute (www.sinano.eu) organizes in Kraków its 15th edition of the SiNANO workshop at ESSDERC-ESSCIRC. The European Roadmap for Nanoelectronics, released in December 2018, shows the high importance of the Heterogeneous Integration for both Academic and Industries. The aim of this workshop will be to present the main results in this domain, particularly focusing on 3D integration, 2D Nanomaterials, MEMS, Neuromorphic and Quantum Computing as well as System Integration. Three sessions are planned: 3D integration methodologies, Integration of new materials, and Applications.

Agenda:
8:00 – 8:30 - Registration
8:30 – 8:45 - Enrico Sangiorgi, Director SiNANO Institute – Presentation of the Workshop
8:45 – 9:15 - Giorgos Fagas, Tyndall – Heterogeneous Integration Roadmap: a System’s Perspective
Session: 3D Integration Methodologies
9:15 – 10:00 - Per-Erik Hellström, KTH – Ge devices for sequential 3D integration
10:00 – 10:30 - Coffee break
10:30 – 11:15 - Aida Todri-Sanial, CNRS LIMM – Physical design and optimisation methods for TSV-based 3D and monolithic 3D integration
11:15 – 12:00 - Fabrice Nemouchi, CEA-Leti – 3D integration the building blocks of upcoming technologies
12:00 – 12:45 - Josef Weber, Fraunhofer, EMFT – Technologies for 3D Heterogeneous System Integration
13:00 – 14:00 - Lunch
Session: Applications
14:00 – 14:45 - Humberto Campanella, Tyndall – Challenges and Opportunities of MEMS for 5G RF Front-end Module integration
14:45 – 15:15 - Giorgos Fagas, Tyndall – Europractice extended Technologies and Services: focus on System Integration
15:30 – 16:00 - Coffee break
Session: Integration of new Materials
16:00 – 16:45 - Ian Povey, Tyndall – Large-area growth of 2D transition metal dichalcogenides by vapour phase methods
16:45 – 17:30 - Georg Duesberg, Uni BW Munich – Low Temperature growth of layered Transition Metal Dichalcogenides for BEOL integration
17:30-18:15 - Max Lemme, AMO – Towards wafer-scale integration of graphene and 2D Materials for electronics, photonics and sensor applications
Workshop details:

Heterogeneous Integration Roadmap: a System’s Perspective
Giorgos Fagas, Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland

ITRS 2.0 contained a comprehensive chapter on Heterogeneous Integration, focusing exclusively on the technology independent of the application pull. The most recent IRDS update discusses the applications in more detail but still does not provide a holistic framework to define Figures of Merit within the system application constraints. It is therefore justified to consider a new approach for road mapping Heterogeneous Integration for System Level Applications. I will present such an innovative roadmap that came out from the NERIEID project – NanoElectronics Roadmap for Europe: Identification and Dissemination – and goes beyond the simple inclusion of static numerical tables. The approach is based on building a general top-down description of the requirements (a hierarchical map) that has to be met in a bottom-up process, with concepts, methods, values and expectations strictly related to the application of reference.

Session 3D Integration Methodologies
Technologies for 3D Heterogeneous System Integration
Josef Weber, Fraunhofer, EMFT

3D Heterogeneous System Integration will become the main challenge for realising miniaturised advanced systems consisting of sensor-, computing-, memory- and communication functionality. Technologies for the integration of MEMS and IC-devices like Fraunhofer EMFT’s TSV-SLID using tungsten-filled vias and Solid-Liquid Interdiffusion (SLID) of Cu/Sn are introduced. Low-temperature bonding technologies for chip-to-wafer and wafer-to-wafer assembly will be presented and assessed with respect to reliability. EMFT’s 3D Foil Assembly Technology enables integration of flexible components on foils, foil-to-foil stacking and development of flexible foil systems. Additionally, Integration of ultra-thin silicon in foils will be demonstrated focusing on RF-applications.

Session Applications
Challenges and Opportunities of MEMS for 5G RF Front-end Module Integration
Humberto Campanello, Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland

The standards for the Fifth Generation of wireless mobile communications New Radio (5G NR), WiFi, and IoT for sub-6GHz operation are demanding more complex RF front-end modules (RF-FEMs) to serve new bands and signal processing schemes that will add to the existing modules and architectures. Such modules are expected to feature combinations of System-in-Package (SiP) and System-on-Chip (SoC) architectures in order to meet the specs for module size, functionality, and manufacturability. Currently, there are gaps at all levels, from functionality, to materials, to manufacturing technologies. This talk will address some of these topics and proposals to close the gaps to build novel RF-FEMs for 5G NR, from the perspective of acoustic MEMS and RFIC integration.
Europractice extended Technologies and Services: Focus on System Integration
Giorgos Fagas, Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland
The mission statement of Europractice is to provide European industry and academia with a platform to develop Electronic Smart Integrated Systems, from advanced prototype design to volume production. The latter will be achieved by providing affordable and easier access to a wide range of state-of-the-art industry-grade fabrication technologies and design tools complemented with training and support to the customer in all critical steps which are needed. It builds on many years’ experience at imec, STFC, FhG-IIS, CMP and Tyndall. Currently, over 600 academic institutes are using these services to train the next generation of engineers for the European industry. In this talk, I will present the overall Europractice services and engagement model, followed by a focused update on the extended services of System Integration beyond the Multi-Project Wafer IC.

Session Integration of new Materials
Low-Temperature Growth of Layered Transition Metal Dichalcogenides for BEOL Integration
Georg S. Duesberg, Institute of Physics, EIT 2, Faculty of Electrical Engineering and Information Technology, Universität der Bundeswehr München, Werner-Heisenberg-Weg 39, 85577 Neubiberg, Germany
Two-dimensional materials such as transition metal dichalcogenides (TMDs) are intensively investigated because of their potential applications in future electronics. So far, mainly group six (Mo/W) TMDs have been investigated, which show thickness depend electronic and optical properties. Metal-to-semiconductor transitions, high mobilities, and high potential for various sensing applications, now have moved the group 10 (Pt/Pd) TMDs or Nobel Metal Dichalcogenides (NMDs) to the center of attention. In this presentation, the low-temperature synthesis of various TMDs by thermally assisted conversion (TAC) is presented. The composition and morphology of the resulting large scale layers are investigated by several characterization techniques including Raman spectroscopy, SPM and X-ray photoelectron spectroscopy. In particular, the low temperature TAC synthesis PtSe₂ potentially allows back end of line (BEOL) integration compatible with silicon technology. The effects of growth on the underlying substrates or investigated by TOF-SIMS and transmission electron microscopy. Further, as pre-patterned structures can be grown by the TAC, which allows fabricating electronic devices using standard micro-fabrication technology. In this regard, examples for high-performance chemical sensors, IR-photodetectors and MEMS devices with PtSe₂ will be presented.
Towards Wafer-Scale Integration of Graphene and 2D Materials for Electronics, Photonics and Sensor Applications

Max Lemme, AMO GmbH, Otto-Blumenthal-Str. 25, 52074 Aachen, Germany

Graphene has been researched intensely over the past 15 years. Its intrinsic electronic and physical properties are unrivaled in many aspects. Hundreds of related two-dimensional (2D) materials with different properties have since been added to the 2D portfolio. Yet, to achieve end-customer products and enter markets in electronics, photonics or sensing, a scalable manufacturing process technology is required. In this talk, I will discuss the major bottlenecks and challenges towards the integration of graphene and 2D materials into semiconductor processing lines. I will also introduce promising device concepts, for which 2D materials clearly could make a difference, such as photodetectors and pressure sensors.
### Tuesday, September 24

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Tuesday, September 24

Joint Plenary 1: Edoardo Charbon, EPFL

Session Code: A1L-A
Location: Main Auditorium A & B
Time: 09:00 - 09:40

09:00 Cryo-CMOS: 60 Years of Technological Advances Towards Emerging Quantum Technologies
Edoardo Charbon
Delft University of Technology, Netherlands

Joint Plenary 2: Franck Arnaud, STMicroelectronics

Session Code: A2L-A
Location: Main Auditorium A & B
Time: 09:40 - 10:20

09:40 28nm FDSOI Platform with Embedded PCM for IoT, ULP, Digital, Analog, Automotive and Others Applications
Franck Arnaud, Sebastien Haendler, Sylvain Clerc, Rossella Ranica, Anna Gandolfo, Olivier Weber
STMicroelectronics, Italy; STMicroelectronics, France
Tuesday, September 24

Focus Session I: Challenges for Power Devices & Merging Microelectronics with Optics

Session Code: A3L-E
Location: Medium Aula A
Time: 11:00 - 12:20
Chair(s): Rainer Pforr; Zeiss

11:00 Double-Sided Cooling Technology for eMobility
Klaus Pressel, Andreas Grassmann, Markus Fink, Günther Tutsch
Infineon Technologies AG, Germany

11:20 Current SiC Power Device Development, Material Defect Measurements and Characterization at Bosch
Daniel Baierhofer
Robert Bosch GmbH, Germany

11:40 Power Packages Interconnections for High Reliability Automotive Applications
Michele Calabretta, Marco Renna, Vincenzo Vinciguerra, Angelo Alberto Messina
STMicroelectronics, Italy

12:00 Pixelated Light: Merging Microelectronics and Photonics
Dominik Scholz, Stefan Groetsch, Michael Wittmann, Alexander Pfeuffer, Martin Strassburg, Andreas Ploessl
OSRAM Opto Semiconductors GmbH, Germany
Tuesday, September 24

WBG and Si Devices for Power and RF

Session Code: A3L-G
Location: Seminar room
Time: 11:00 - 12:20
Chair(s): Mikael Östling; KTH
Florian Udrea; Cambridge University, UK

11:00 Impact of Channel Length on Characteristics of 600V 4H-SiC Inversion-Channel Planar MOSFETs
Aditi Agarwal, Kijeong Han, B. Jayant Baliga
North Carolina State University, United States

11:20 Characterization and Modeling of BTI in SiC MOSFETs
Davide Cornigli², Andrea Tallarico², Susanna Reggiani², Claudio Fiegnia², Enrico Sangiorgi², Luis Sanchez¹, Carlos Valdivieso¹, Giuseppe Consentino¹, Felice Crupi¹
¹Università della Calabria, Italy; ²Università di Bologna, Italy

11:40 TCAD Predictions of Hot-Electron Injection in p-Type LDMOS Transistors
Federico Giuliano², Andrea Tallarico², Susanna Reggiani², Antonio Gnudi², Enrico Sangiorgi², Claudio Fiegnia², Mattia Rossetti¹, Antonio Molfese¹, Stefano Manzini¹, Riccardo Depetro¹, Giuseppe Croce¹
¹STMicroelectronics, Italy; ²Università di Bologna, Italy

12:00 Electrical and Noise Characteristics of Fin-Shaped GaN/AlGaN Devices for High Frequency Operation
Pavlo Sai³, Dmytro But³, Maksym Dub³, Maciej Sakowicz¹, Bartlomiej Grzywacz¹, Pawel Prystawko¹, Grzegorz Cywiński³, Wojciech Knap³, Sergey Rumyantsev¹
¹Institute of High Pressure Physics PAS, Poland; ²Institute of High Pressure Physics PAS / ISP NASU, Poland; ³Institute of High Pressure Physics PAS / Warsaw University of Technology, Poland; ⁴Institute of High Pressure Physics PAS / Warsaw University of Technology / University of Montpellier, Poland
**Tuesday, September 24**

**Focus Session II: MEMS, Sensors & Advanced Integration Technologies**

Session Code: A4L-E  
Location: Medium Aula A  
Time: 14:00 - 15:20  
Chair(s): Klaus Pressel; *Infineon Technologies*

**14:00**  
**Bosch MEMS Foundry Service**  
Stefan Majoni  
*Bosch, Germany*

**14:20**  
**Micro-Transfer-Printing – a Unique Technology for Heterogeneous Integration of (Opto-) Electronic Components**  
Gabriel Kittler  
*X-FAB Semiconductor Foundries GmbH, Germany*

**14:40**  
**Silicon Photomultipliers Technology at Fondazione Bruno Kessler and 3D Integration Perspectives**  
Giovanni Paternoster, Lorenza Ferrario, Fabio Acerbi, Alberto Gola, Pierluigi Bellutti  
*Fondazione Bruno Kessler, Italy*

**15:00**  
**Challenges and Capabilities of 3D Integration in CMOS Imaging Sensors**  
Dominique Thomas, Jean Michailos, Krysten Rochereau  
*STMicroelectronics, France*
Tuesday, September 24

Compact Modeling Under Cryogenic Conditions

Session Code: A4L-G
Location: Seminar room
Time: 14:00 - 15:20
Chair(s): Thierry Poiroux; CEA-LETI
Benjamin Iñiguez; University Rovira i Virgili

14:00 Cryogenic MOSFET Threshold Voltage Model
Arnout Beckers, Farzan Jazaeri, Christian Enz
École Polytechnique Fédérale de Lausanne, Switzerland

14:20 Subthreshold Mismatch in Nanometer CMOS at Cryogenic Temperatures
Pascal Alexander ’t Hart1, Masoud Babaie1, Edoardo Charbon1, Andrei Vladimirescu2, Fabio Sebastianio1
1Delft University of Technology, Netherlands; 2University of California, Berkeley, United States

14:40 Test Chip for Identifying Spice-Parameters of Cryogenic BiFET Circuits
Oleg Dvornikov5, Nikolay Prokopenko4, Vladimir Tchekhovski1, Yaroslav Galkin2, Alexei Kunz2, Anna Bugakova3
1Belarusian State University, Belarus; 2Belarusian State University of Informatics and Radioelectronics, Belarus; 3Don State Technical University, Russia; 4Don State Technical University, Institute for Design Problems in Microelectronics of RAS, Russia; 5Minsk Research Instrument-Making Institute JSC, Belarus
Tuesday, September 24

ESSDERC Keynote 1: Michael Heuken, AIXTRON AG

Session Code: A5L-B
Location: Main Auditorium B
Time: 15:50 - 16:30

15:50 GaN Based HEMT Technology for Power and RF Applications
Michael Heuken
AIXTRON SE, Germany
Tuesday, September 24

Focus Session III: Advanced Semiconductor Process & Device Technologies in Europe

Session Code: A6L-E
Location: Medium Aula A
Time: 16:40 - 18:00
Chair(s): Dominique Thomas; STMicroelectronics

16:40 Excursion Prevention and Increasing Device Performance Using Mask Correction for Intrafield CD and Overlay Improvement
Thomas Scherübl, Yael Sufrin, Avi Cohen, Ofir Sharoni, Rolf Seltmann
Carl Zeiss SMT GmbH, Germany

17:00 High-NA EUV Optics – the Key for Miniaturization of Integrated Circuits in the Next Decade
Heiko Feldmann, Paul Gräupner, Peter Kürz, Winfried Kaiser
Carl Zeiss SMT GmbH, Germany

17:20 22FD-SOI Variability Improvement Thanks to SmartCut Thickness Control at Atomic Scale
Soitec, France

Sebastian Höppner2, Holger Eisenreich2, Dennis Walter2, Uwe Steeb2, Andre Scharfe2, Clifford Dmello2, Robert Sinkwitz2, Heiner Bauer2, Alexander Oefelein2, Florian Schraut2, Jörg Schreiter2, Robert Niebsch2, Stephan Scherzer2, Mario Orgis2, Ulrich Hensel1, Jörg Winkler1
1Globalfoundries, Germany; 2Racyics GmbH, Germany

18:00 22FDX™ Technology and Add-on-Functionalities
Maciej Wiatr, Sabine Kolodinski
Globalfoundries, Germany

18:20 IPCEI Subcontracts Contributing to 22-FDX Add-on Functionalities at GF
1Fraunhofer Institute for Photonic Microsystems, Germany; 2Globalfoundries, Germany; 3NaMLab gGmbH, Germany; 4Technische Universität Dresden, Germany
Tuesday, September 24

FET Devices for Sensing Applications

Session Code: A6L-G
Location: Seminar room
Time: 16:40 - 18:00
Chair(s): Volker Cimalla; Fraunhofer IAF
Clara Moldovan; EPFL

16:40 Monolithically Integrated Catalyst-Free High Aspect Ratio InAs-On-Insulator (InAsOI) FinFETs for pH Sensing
Maneesha Rupakula¹, Junrui Zhang¹, Francesco Bellando¹, Fabien Wildhaber³, Clarissa Convertino³, Heinz Schmid², Kirsten Moselund³, Adrian Ionescu¹
¹École Polytechnique Fédérale de Lausanne, Switzerland; ²IBM Zurich Research Laboratory, Switzerland; ³Xsensio S.A, Switzerland

17:00 The Module of Gain-Controllable Amplifier Readout Circuits Based on Si Nanowire ISFET for Biochips for Optimization of Dynamic Range, Linearity, and Resolution
Sungju Choi, Jungmok Kim, Jinsu Yoon, Inseok Chae, Sung-Jin Choi, Dong Myong Kim, Hyun-Sun Mo, Dae Hwan Kim
Kookmin University, Korea

17:20 49dB Depletion-Load Amplifiers with Polysilicon Source-Gated Transistors
Eva Bestelink², Ravi Silva², Radu Sporea², Luca Maiolo¹, Francesco Maita¹
¹Consiglio Nazionale delle Ricerche, Italy; ²University of Surrey, United Kingdom
Wednesday, September 25

Joint Plenary 3: Toshio Yanagida, Osaka University

Session Code: B1L-A
Location: Main Auditorium A & B
Time: 09:00 - 09:40

09:00 Single Molecule Nano-Science: Noise and Function of Life
Toshio Yanagida
Osaka University, Japan
Wednesday, September 25

Advanced and Emerging Memories

Session Code: B2L-E
Location: Medium Aula A
Time: 10:20 - 12:00
Chair(s): Andrea Lacaita; Politecnico di Milano, Italy
Kensuke Ota; Toshiba Memory, Japan

10:20 Ultra-Dense co-Integration of FeFETs and CMOS Logic Enabling Very-Fine Grained Logic-in-Memory
Evelyn Tina Breyer2, Halid Mulaosmanovic2, Jens Trommer2, Thomas Melde1, Stefan Dünkel1, Martin Trentsch1, Sven Beyer1, Thomas Nikolajick3, Stefan Slesazeck2
1Globalfoundries Fab1 LLC & Co. KG, Germany; 2NaMLab gGmbH, Germany; 3NaMLab gGmbH and Technische Universität Dresden, Germany

10:40 Impact of Program Accuracy and Random Telegraph Noise on the Performance of a NOR Flash-Based Neuromorphic Classifier
Gerardo Malavena, Simone Petrò, Alessandro Sottocornola Spinelli, Christian Monzio Compagnoni
Politecnico di Milano, Italy

11:00 Joule Heating in SiOx RRAM Device Studied by an Integrated Micro-Thermal Stage
Nicola Polino, Mario Laudato, Elia Ambrosi, Alessandro Bricalli, Daniele Ielmini
Politecnico di Milano, Italy

11:20 SIMPLY: Design of a RRAM-Based Smart Logic-in-Memory Architecture Using RRAM Compact Model
Francesco Maria Puglisi, Tommaso Zanotti, Paolo Pavan
Università di Modena e Reggio Emilia, Italy
Non-Conventional Devices

Session Code: B2L-F
Location: Medium Aula B
Time: 10:20 - 12:00
Chair(s): Gianluca Fiori; University of Pisa
Tibor Grasser; TU Wien

10:20 Eliminating Charge Sharing in Clocked Logic Gates on the Device Level Employing Transistors with Multiple Independent Inputs
Jens Trommer¹, Maik Simon¹, Stefan Slesazeck¹, Walter Michael Weber¹, Thomas Mikolajick²
¹NaMLab gGmbH, Germany; ²NaMLab gGmbH and Technische Universität Dresden, Germany

10:40 Large Scale MoS₂/Si Photodiodes with Graphene Transparent Electrodes
Melkamu Belete³, Satender Kataria³, Sarah Riazimehr³, Gunther Lippert², Mindaugas Lukosius², Daniel Schneider¹, Andreas Bablich³, Olof Engström¹, Max Christian Lemme⁴
¹AMO GmbH, Germany; ²Leibniz-Institut für innovative Mikroelektronik, Germany; ³RWTH Aachen University, Germany; ⁴RWTH Aachen University and AMO GmbH, Germany; ⁵Universität Siegen, Germany

11:00 Si-Based Spin Metal-Oxide-Semiconductor Field-Effect Transistors with an Inversion Channel
Ryosho Nakane, Shoichi Sato, Masaaki Tanaka
University of Tokyo, Japan

11:20 Switching Speedup of the Magnetic Free Layer of Advanced SOT-MRAM
Roberto Lacerda de Orio², Alexander Makarov², Siegfried Selberherr², Wolfgang Goes¹, Johannes Ender², Simone Fiorentini², Viktor Sverdlov²
¹Silvaco Europe Ltd, United Kingdom; ²Technische Universität Wien, Austria
Wednesday, September 25

Modeling of Compound Semiconductor Devices

Session Code: B2L-G
Location: Seminar room
Time: 10:20 - 12:00
Chair(s): Benjamin Iñiguez; University Rovira i Virgili
Wladek Grabinski; MOS-AK, Switzerland

10:20 First Uni-Traveling Carrier Photodiode Compact Model Enabling Future Terahertz Communication System Design
Chhandak Mukherjee1, Patrick Mounaix1, Cristell Maneux1, Michele Natrella2, James Seddon2, Chris Graham2, Cyril C. Renaud2
1Université de Bordeaux, France; 2University College London, United Kingdom

10:40 Impact of SiGe HBT Hot-Carrier Degradation on the Broadband Amplifier Output Supply Current
Marine Couret2, Gerhard Fischer1, Iria Garcia-Lopez1, Magali De Matos2, François Marc2, Cristell Maneux2
1Leibniz-Institut für innovative Mikroelektronik, Germany; 2Université de Bordeaux, France

11:00 Monolithically Integrated GaN Power ICs Designed Using the MIT Virtual Source GaNFET (MVSG) Compact Model for Enhancement-Mode p-GaN Gate Power HEMTs, Logic Transistors and Resistors
Shuzhen You2, Xiangdong Li2, Stefaan Decoutere2, Guido Groeseneken2, Zhanfei Chen1, Jun Liu1, Yuki Yamashita3, Kazutoshi Kobayashi3
1Hangzhou Dianzi University, China; 2IMEC, Belgium; 3Kyoto Institute of Technology, Japan
13:30 The N3XT 1,000X for the Coming Superstorm of Abundant Data: Carbon Nanotube FETs, Resistive RAM, Monolithic 3D
Subhasish Mitra
Stanford University, United States
Wednesday, September 25

Analog/RF

Session Code: B4L-E  
Location: Medium Aula A  
Time: 14:20 - 15:40  
Chair(s): Gunnar Malm; KTH  
Nadine Collaert; IMEC

14:20  **Self-Heating in 28 FDSOI UTBB MOSFETs at Cryogenic Temperatures**  
Lucas Nyssens², Arka Halder², Babak Kazemi Esfeh², Nicolas Planes¹, Michel Haond¹, Denis Flandre², Jean-Pierre Raskin², Valeriya Kilchytska²  
¹STMicroelectronics, France; ²Université catholique de Louvain, Belgium

14:40  **22FDX® fMAX Optimization Through Parasitics Reduction and GM Boost**  
Zhixing Zhao², Steffen Lehmann², Luca Lucci¹, Yogadissen Andee², Alexis Divay¹, Luca Pirro², Tom Herrmann², Alban Zaka², Ricardo Sousa¹, Patrick James Artz², Klaus Hempel², Juergen Faul², Tianbing Chen², Richard Taylor², Jerome Mazurier², Carsten Grass², Jan Hoentschel², David Harame²  
¹CEA LETI, France; ²Globalfoundries, Germany

15:00  **Demonstration and Modelling of Excellent RF Switch Performance of 22nm FD-SOI Technology for Millimeter-Wave Applications**  
Shon Yadav, Abdellatif Bellaouar, Jen Shuang Wong, Tianbing Chen, Satoshi Sekine, Christoph Schwan, Mei See Chin, Glenn Workman, Kok Wai Chew, Wai Heng Chow  
Globalfoundries, Germany; Globalfoundries, India; Globalfoundries, Singapore; Globalfoundries, United States
Wednesday, September 25

Hardware for Neuromorphic Computing

Session Code: B4L-F
Location: Medium Aula B
Time: 14:20 - 15:40
Chair(s): Siegfried Karg; IBM
Max Lemme; RWTH Aachen University

14:20 Low-Energy Inference Machine with Multilevel HfO2 RRAM Arrays
Valerio Milo², Cristian Zambelli³, Piero Olivo³, Eduardo Pérez¹, Oscar Gonzalez Ossorio⁴, Christian Wenger¹, Daniele Ielmini²
¹Leibniz-Institut für innovative Mikroelektronik, Germany; ²Politecnico di Milano, Italy; ³Università di Ferrara, Italy; ⁴University of Valladolid, Spain

14:40 Parallel Product-Sum Operation Neuromorphic Systems with 4-Bit Ferroelectric FET Synapses
Koki Kamimura, Susumu Nohmi, Kenta Suzuki, Ken Takeuchi
Chuo University, Japan
Wednesday, September 25

Advances in MOSFET Modeling

Session Code: B4L-G
Location: Seminar room
Time: 14:20 - 15:40
Chair(s): Daniel Tomaszewski; ITE Warsaw
Thierry Poiroux; CEA-LETI

14:20 The Synergy SPICE – Compact Models
Andrei Vladimirescu
University of California, Berkeley, United States

14:40 Comparison of Modeling Approaches for Transistor Degradation: Model Card Adaptations Vs Subcircuits
André Lange¹, Fabio A. Velarde Gonzalez¹, Insaf Lahbib³, Sonja Crocoli²
¹Fraunhofer Institute for Integrated Circuits IIS/EAS, Germany;
²X-FAB Dresden GmbH & Co. KG, Germany;
³X-FAB France SAS, France

15:00 FOSS EKV2.6 Verilog-A Compact MOSFET Model
Wladek Wladek Grabinski¹⁰, Marcelo Pavanello¹, Michelly de Souza¹, Daniel Tomaszewski⁸, Jola Malesinska⁸, Grzegorz Gliuszek⁸, Matthias Bucher¹¹, Nikolaos Makris¹¹, Aristeidis Nikolaou¹¹, Ahmed Abo-Elhadid⁹, Marek Mierzwniski¹², Laurent Lemaitre⁶, Mike Brinson⁷, Christophe Lallement¹³, Jean-Michel Sallesse¹, Sadayuki Yoshitomi¹², Paul Malisse⁴, Henri Oguey², Stefan Cservény², Christian Enz¹, François Krummenacher¹, Eric Vittoz³
¹Centro Universitário FEI, Brazil; ²CSEM SA, Switzerland;
³École Polytechnique Fédérale de Lausanne, Switzerland;
⁴Europractice/IMEC, Belgium; ⁵Keysight Technologies, United States; ⁶Lemaitre EDA Consulting, France; ⁷London Metropolitan University, United Kingdom; ⁸UKASIEWICZ Institute of Electron Technology, Poland; ⁹Mentor Graphics, United States; ¹⁰MOS-AK Association, Switzerland; ¹¹Technical University of Crete, Greece; ¹²Toshiba Corporation, Japan;
¹³Université de Strasbourg, France
Thursday, September 26

Joint Plenary 4: Donhee Ham, Harvard University

Session Code: C1L-A
Location: Main Auditorium A & B
Time: 09:00 - 09:40

09:00 CMOS Interface with Biological Molecules and Cells
Jeffrey Abbott, Tianyang Ye, Hongkun Park, Donhee Ham
Harvard University, United States
Thursday, September 26

Modeling of Trap Effects and Noise

Session Code: C2L-E
Location: Medium Aula A
Time: 10:20 - 12:00
Chair(s): Sadayuki Yoshitomi; Toshiba
Daniel Tomaszewski; ITE Warsaw

10:20 Compact Analytical Model for Trap-Related Low Frequency Noise in Junctionless Transistors
Renan Trevisoli³, Rodrigo Doria², Sylvain Barraud¹, Marcelo Pavanello²
¹CEA LETI, France; ²Centro Universitário FEI, Brazil;
³Universidade Federal do ABC, Brazil

10:40 Compact Modeling of Low Frequency Noise and Thermal Noise in Junction Field Effect Transistors
Nikolaos Makris, Loukas Chevas, Matthias Bucher
Technical University of Crete, Greece

11:00 Evaluation of Static/Transient Performance of TFET Inverter Regarding Device Parameters Using a Compact Model
Atieh Farokhnejad¹, Fabian Horst¹, Benjamin Iñíguez², Francois Lime², Alexander Kloes¹
¹TH Mittelhessen University of Applied Sciences, Germany;
²Universitat Rovira i Virgili, Spain
Thursday, September 26

Photonic and Microwave Devices

Session Code: C2L-F
Location: Medium Aula B
Time: 10:20 - 12:00
Chair(s): Dana Cristea; IMT Bucharest
Susanna Reggiani; University of Bologna

10:20 Design and Characterization of Monolithic Microring Resonator Based Photodetector in 45nm SOI CMOS
Nandish Mehta, Sidney Buchbinder, Vladimir Stojanović
University of California, Berkeley, United States

10:40 Body-Biasing Considerations with SPAD FDSOI: Advantages and Drawbacks
Tulio Chaves de Albuquerque2, Dylan Issartel2, Raphael Clerc4, Patrick Pillet2, Remy Cellier2, Wilfried Uhring3, Andreia Catelin1, Francis Calmon2
1STMicroelectronics, France; 2Université de Lyon, France; 3Université de Strasbourg, France; 4Université Jean Monnet & Institut d’Optique Graduate School, France

11:00 Highly Sensitive p-GaAsSb/n-InAs Nanowire Backward Diodes for Low-Power Microwaves
Tsuyoshi Takahashi1, Kenichi Kawaguchi1, Masaru Sato1, Michihiko Suhara2, Naoya Okamoto1
1Fujitsu Limited and Fujitsu Laboratories Ltd., Japan; 2Tokyo Metropolitan University, Japan

11:20 DC-110 GHz Characterization of 22FDX® FDSOI Transistors for 5G Transmitter Front-End
Quang Huy Le1, Dang Khoa Huynh1, Defu Wang1, Thomas Kämpe1, Steffen Lehmann2
1Fraunhofer Institute for Photonic Microsystems, Germany; 2Globalfoundries, Germany
Thursday, September 26

Multi-physics Modeling

Session Code: C2L-G
Location: Seminar room
Time: 10:20 - 12:00
Chair(s): Zlatan Stanojevic; Global TCAD Solutions, Austria
Viktor Sverdlov; TU Wien, Austria

10:20 Current Transport in Polysilicon-Channel GAA MOSFETs: a Modeling Perspective
Aurelio Mannara, Alessandro Sottocornola Spinelli, Andrea
Leonardo Lacaita, Christian Monzio Compagnoni
Politecnico di Milano, Italy

10:40 Investigations on Current Filamentation in PiN Diodes Using TLP Measurements and TCAD Simulations
Patrick Scharf1, Christoph Sohrmann1, Steffen Holland2, Volkhard Beyer1
1Fraunhofer Institute for Integrated Circuits IIS/EAS, Germany;
2Nexperia Germany GmbH, Germany

11:00 A Fast Method for Modeling and Optimizing Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors
Federico Pace4, Olivier Marcelot3, Philippe Martin-Gonthier3, Olivier Saint-Pé1, Michel Breart de Boisanger1, Rose-Marie
Sauvage2, Pierre Magnan3
1Airbus, France; 2Direction Générale de l'Armement, France;
3Université de Toulouse, France; 4Université de Toulouse and
Airbus Defence & Space, France
Thursday, September 26

ESSDERC Keynote 3: Jong-Ho Lee, Seoul National University

Session Code: C3L-B
Location: Main Auditorium B
Time: 13:30 - 14:10

13:30 Review of Candidate Devices for Neuromorphic Applications
Jong-Ho Lee, Sung Yun Woo, Sung-Tae Lee, Suhwan Lim, Won-Mook Kang, Young-Tak Seo, Soochang Lee, Dongseok Kwon, Seongbin Oh, Yoo hyun Noh, Hyeongsu Kim, Jangsaeng Kim, Jong-Ho Bae
Seoul National University, Korea
Thursday, September 26

Derivative Technologies

Session Code: C4L-E
Location: Medium Aula A
Time: 14:20 - 15:40
Chair(s): Francois Andrieu; CEA-LETI
Blandine Duriez; TSMC

Andrea Vici², Felice Russo¹, Nicola Lovisi¹, Aldo Marchioni¹, Antonio Casella¹, Fernanda Irrera²
¹LFoundry, Italy; ²Sapienza University of Rome, Italy

14:40  Temperature and Gate Leakage Influence on the Z²-FET Memory Operation
Carlos Marquez³, Santiago Navarro³, Carlos Navarro³, Norberto Salazar³, Philippe Galy², Sorin Cristoloveanu¹, Francisco Gamiz³
¹Grenoble Institute of Technology, France; ²STMicroelectronics, France; ³University of Granada, Spain

15:00  Back-end-of-Line CMOS-Compatible Diode Fabrication with Pure Boron Deposition Down to 50 °C
Tihomir Knežević¹, Tomislav Suligoj³, Xingyu Liu², Lis K. Nanver², Ahmed Elsayed¹, Jan F. Dick¹, Joerg Schulze¹
¹Universität Stuttgart, Germany; ²University of Twente, Netherlands; ³University of Zagreb, Croatia
Optical and Thermal Sensors

Session Code: C4L-F
Location: Medium Aula B
Time: 14:20 - 15:40
Chair(s): Joachim Burghartz; IMS CHIPS
Mirjana Banjevic; Sensirion AG

14:20 A Novel 4H-SiC UV Photo-Transistor Based on a Shallow Mesa Structure
Luigi Di Benedetto, Gian Domenico Licciardo, Alfredo Rubino
Università degli Studi di Salerno, Italy

14:40 Low-Noise and High-Efficiency Near-IR SPADs in 110nm CIS Technology
Ion Vornicu, Franco Bandi, Ricardo Carmona-Galán, Angel Rodríguez-Vázquez
IMSE-CNMC Universidad de Sevilla, Spain

15:00 Photonic Thermal Sensor Integration Towards Electronic-Photonic-IC Technologies
Andreas Mai², Siegfried Bondarenko³, Christian Mai¹, Patrick Steglich²
¹Leibniz-Institut für innovative Mikroelektronik, Germany;
²Leibniz-Institut für innovative Mikroelektronik and Technische Hochschule Wildau, Germany;
³Technische Hochschule Wildau, Germany

15:20 Suspended Antenna-Coupled Nanothermocouple Array for Long-Wave Infrared Detection
Gergo Szakmany, Gary Bernstein, Alexei Orlov, Wolfgang Porod
University of Notre Dame, United States
Thursday, September 26

Advanced Device Modeling

Session Code: C4L-G
Location: Seminar room
Time: 14:20 - 15:40
Chair(s): Demins Rideau; STMicroelectronics, France
Aryan Afzalian; TSMC, Taiwan

14:20 Stochastic Modeling of Hot-Carrier Degradation in nFinFETs Considering the Impact of Random Traps and Random Dopants
Alexander Makarov², Ben Kaczer¹, Philippe Roussel¹, Adrian Chasin¹, Michiel Vandemaele¹, Geert Hellings¹, Al-Moatasem El-Sayed², Markus Jech², Tibor Grasser², Dimitri Linten¹, Stanislav Tyaginov¹
¹IMEC, Belgium; ²Technische Universität Wien, Austria

14:40 On the Electron Mobility of Strained InGaAs Channel MOSFETs
Stefania Carapezzi, Susanna Reggiani, Elena Gnani, Antonio Gnudi
Università di Bologna, Italy

15:00 Circuit-Based Hydrodynamic Modeling of AlGaN/GaN HEMTs
Florian Ludwig², Maris Bauer¹, Alvydas Liasuskas³, Hartmut Roskos²
¹Fraunhofer Institute for Mechanics of Materials, Germany; ²Johann Wolfgang Goethe-Universität, Germany; ³Vilnius University, Lithuania
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