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CONTACT

LOCAL SCIENTIFIC SECRETARIAT

Krzysztof Kasinski (AGH UST, PL)
Robert Szczygiel (AGH UST, PL)

ORGANIZING SECRETARIAT

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+48 12 617 46 04 | kf@agh.edu.pl

PLANNED TUTORIALS AND WORKSHOPS

Nanoscale Technology, Transistor Modeling & IC Design
Chairs: Wladek Grabiński (GMC, CH),
Daniel Tomaszewski (ITE, PL)

Circuits and Systems Enabling Quantum Technologies
Chair: Edoardo Charbon (EPFL Lausanne, CH)

5G Radios: Concepts, Systems, and Silicon
Chairs: Gernot Hubert (Silicon Austria Labs, AT),
Francois Rivet (IMS Bordeaux, FR)

Low-power RF and Analog Circuits
Chairs: Masoud Babaie (TU Delft, NL),
Teerachot Siriburanon (UCD Dublin, IE)

Basics of Jitter and Phase Noise
Chair: Ali Sheikholeslami (University of Toronto, CA)

THz Science, Technologies and Applications
Chair: Wojciech Knap (PAS, PL & CNRS, FR)

Technologies and Devices for IoT
Chair: Adrian Ionescu (EPFL, CH)

CONFERENCE VENUE

- The conference venue will be in the strict center of Cracow in the Auditorium Maximum of Jagiellonian University.

- **ESSDERC/ESSCIRC** Gala Dinner on Wednesday, Sept. 25, 2019 will be held in Wieliczka Salt Mine (UNESCO).

Diamond Sponsor

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CRACOW - THE CITY OF KINGS

The magical city of Cracow is the second largest city in Poland. Located in the south of the country on the Vistula river, it is a capital city of Lesser Poland Voivodeship. It is a place where history and tradition intertwine with culture, modern technologies and economic development.

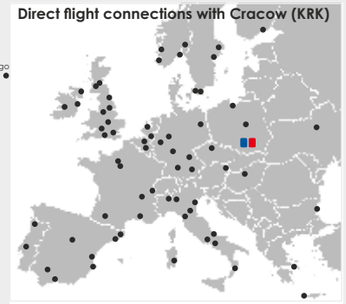
Officially rooted in XIIIth century, its history is much older. Being the capital of the Crown of the Kingdom of Poland between 1038 and 1569, it has never stopped thriving as an economic and cultural center. Cracow's Golden Age came by the end of the 15th century when it was the thriving metropolis of a vast and prosperous kingdom stretching from the Black Sea to the Baltic Sea.

The uniqueness of this place has not gone unnoticed. Entire Cracow's Historic Centre (Old Town) is on the UNESCO World Heritage List. It is recognized by many by its largest medieval market square in Europe and its architecture originating from Gothic through Renaissance and Baroque epochs. The Royal Wawel Castle, the seat of Polish kings and their biggest necropolis, is a diamond that rules over the landscape of the city. It was officially recognized as European Capital of Culture (2000), UNESCO City of Literature (2012) and hosted World Youth Days (2016) as well as participated in European Football Championship (2012).

Another important feature of Cracow is its academical prowess. With over 650 years of academic tradition, it holds one of the oldest civil universities in Europe (Jagiellonian University). Currently it is a home to five major universities (with AGH University of Science and Technology leading in engineering research) and various higher education school, which gives a total population of approximately 200 thousand students.

The high-tech landscape in Cracow continues to expand. It boast a special economic zone (Cracow Technological Park for major high-tech investments) with several major R&D centers (e.g. Motorola, ABB, Nokia, Aptiv, Silicon Creations, Ericsson, Comarch) focused on industrial electronics and software, four enterprise incubators, three commercial-fair grounds, and seven higher schools of economics. Over 100,000 private businesses and nearly 2,000 public firms carry on in Cracow with an aggregate revenue to the tune of 14.6 billion euro. Surprisingly, the city's big companies with hundreds and thousands on the payroll come under the spotlight yet they are hardly representative of Cracow's economy. The self-employed and small enterprises employing less than ten workers account for over ninety percent of business entities incorporated in the city. Foreigners own (wholly or partially) more than 1,900 of Cracow's companies."

Direct flight connections with Cracow (KRK)



2nd CALL for PAPERS

IEEE | SSCS | ELECTRON DEVICES SOCIETY

WWW.ESSCIRC-ESSDERC2019.ORG

AGH Warsaw University of Technology | CEZAMAT | Jagiellonian University in Kraków

GENERAL PURPOSE OF THE CONFERENCE

The aim of **ESSDERC** and **ESSCIRC** is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary. While keeping separate Technical Program Committees, **ESSDERC** and **ESSCIRC** are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

KEYNOTE SPEAKERS

Joint ESSDERC / ESSCIRC Keynotes:

- **Edoardo Charbon** (EPFL, CH)
  Cryo-CMOS: 60 Years of Technological Advances towards Emerging Quantum Technologies
- **Donhee Ham** (Harvard University, US)
  Copying brain with semiconductor technology
- **Toshio Yanagida** (Osaka University, JP)
  Single Molecule Nano-Science: Noise and Function of Life
- **Franck Arnaud** (STMicroelectronics)
  28nm FDSOI platform with embedded PCM for IoT, ULP, digital, analog, automotive and other applications

ESSDERC Keynotes:

- **Michael Heuken** (AIXTRON AG, GE)
  GaN based HEMT technology for power and RF applications
- **Jong-Ho Lee** (Seoul National University,KR)
  Review of promising devices for neuromorphic applications
- **Subhasish Mitra** (Stanford University, US)
  The N3XT 1,000X for the Coming Superstorm of Abundant Data: Carbon Nanotube FETs, Resistive RAM, Monolithic 3D

ESSCIRC Keynotes:

- **Pieter Harpe** (TU Eindhoven, NL)
  Low-power SAR ADCs: trends, examples and future
- **Ram K. Krishnamurthy** (Intel, US)
  Machine learning and hardware security technologies for the IoT era: Challenges and Opportunities
- **Jeff Walling** (Tyndall National Institute, IE)
  Leveraging the Switched Capacitor Power Amplifier for Future Communications Systems

CONFERENCE TOPICS

Although not limited, papers are solicited for the following main topics:

ESSDERC

- **CMOS Devices and Technology**
- **Opto-, Power and Microwave Devices**
- **Sensor Devices and Technology**
- **Physical Modeling of Materials and Devices**
- **Compact Modeling of Devices and Circuits**
- **Memory Devices and Technology**
- **Emerging non-CMOS Devices and Technologies**

ESSCIRC

- **Analog**
- **Data Converters**
- **RF and mm-Wave**
- **Frequency Generation**
- **Wireless and Wireline Systems**
- **Sensors, Imager and Biomedical**
- **Digital, Security and Memory**
- **Power Management**

CRACOW 2019
ESSDERC
ESSCIRC

PAPER SUBMISSION

Conference proceedings in
IEEE Xplore

All accepted ESSDERC and ESSCIRC papers will be included in the conference proceedings and posted on IEEE Xplore after the conference.

Co-publication of qualified papers in:

Special issue of
IEEE Solid-State Circuits Letters (SSC-L)

Upon acceptance, outstanding ESSCIRC papers will be invited to submit to a Special Issue of IEEE Solid-State Circuit Letters (SSC-L, 4 pages format) on the ESSCIRC, subject to additional editorial and quality reviews. The SSC-L Special Issue is synchronized to the ESSCIRC, and published on IEEE Xplore in September 2019.

Special issue of
IEEE Journal of Solid-State Circuits (JSSC)

Authors of outstanding papers will be invited to submit their work to a Special Issue of IEEE Journal of Solid-State Circuits (JSSC, up to 10-12 pages format) on the ESSCIRC to appear in July 2020, with an opportunity to provide additional material, such as mathematical analysis, in-depth circuit description, more experimental results and benchmarking data. **Publication of a 4-page paper in the SSC-L Special Issue does not preclude invitation to submit an extended version to the JSSC, or invitation to the JSSC Special Issue.**

Special issue of
IEEE Journal of the Electron Devices Society (J-EDS)

Authors of selected outstanding ESSDERC papers will be invited to submit their work to the special issue of IEEE Journal of the Electron Devices Society. The authors will be asked to revise the conference version of the paper by adding at least 30% new material. All manuscripts will undergo additional editorial and quality review process.

PAPER SUBMISSION

Manuscript guidelines as well as instructions on how to submit electronically will be available on the conference website. Papers must not exceed four A4 pages with all illustrations and references included.

All submissions must be received by 8th April 2019.

Papers submitted for review must clearly state:

- The purpose of the work
- How and to what extent it advances the state-of-the art
- Specific results and their impact

Only work that has not been previously published or submitted elsewhere will be considered.
Submission of a paper for review and subsequent acceptance is considered as a commitment that the work will not be publicly available prior to the conference.

After selection of papers, the authors will be informed about the decision of the Technical Program Committee by e-mail by 31th May 2019.

At the same time, the complete program will be published on the conference website. An oral presentation will be given at the Conference for each accepted paper. No-shows will result in the exclusion of the papers from any conference related publication. The submitted final PDF files should be IEEE Xplore compliant.

For each paper independently, at least one co-author is required to register for the Conference (one registration-one paper policy).

Registration fees and deadlines will be available on the conference website.

The working language of the conference is English.

BEST PAPER AWARD

Papers presented at the conference will be considered for the „Best Paper Award" and „Best Young Scientist Paper Award" based on the results of the paper selection process and the judgment of the conference participants. The award ceremony will take place during next **ESSDERC**/**ESSCIRC**, in 2020.