CONFERENCE HIGHLIGHTS

- 4 joint keynote presentations
- 3 **ESSDERC** keynote presentations
- 3 **ESSCIRC** keynote presentations
- Invited papers with overall coverage of all aspects of advanced devices and circuits
- Presentation of IEEE and **ESSDERC**/**ESSCIRC** 2018 Awards
- **ESSDERC**/**ESSCIRC** Gala Dinner on Wednesday, Sept. 25, 2019

- **Planned Tutorials and Workshops:**

Nanoscale Technology, Transistor Modeling & IC Design
Chair: Wladek Grabiński (GMC, CH)

Circuits and Systems Enabling Quantum Technologies
Chair: Edoardo Charbon (EPFL Lausanne, CH)

5G Radios: Concepts, Systems, and Silicon
Chairs: Gernot Hubert (Silicon Austria Labs, AT),
Francois Rivet (IMS Bordeaux, FR)

Low-power RF and Analog Circuits
Chairs: Masoud Babaie (TU Delft, NL),
Teerachot Siriburanon (UCD Dublin, IE)

Basics of Jitter and Phase Noise
Chair: Ali Sheikholeslami (University of Toronto, CA)

THz Science, Technologies and Applications
Chair: Wojciech Knap (PAS, PL & CNRS, FR)

Technologies and Devices for IoT
Chair: Adrian Ionescu (EPFL, CH)

The venue of the conference events will be in the strict centre of Cracow in the Auditorium Maximum of Jagiellonian University.

The working language of the conference is English.

BEST PAPER AWARD

Papers presented at the conference will be considered for the „Best Paper Award" and „Best Young Scientist Paper Award". The selection will be based on the results of the paper selection process and the judgment of the conference participants. The award delivery will take place during **ESSDERC**/**ESSCIRC** 2020.

ORGANIZING COMMITTEE

Pawel Grybos (AGH UST, PL)	General Chair
Maciej Ogorzalek (Jagiellonian University, PL)	General Co-Chair
Thomas Ernst (CEA-LETI, FR)	General Vice-Chair

ESSDERC TPC

Tomasz Skotnicki (CEZAMAT, PL)	TPC Chair
Romuald Beck (WUT, PL)	TPC Co-Chair
Francois Andrieu (LETI, FR)	TPC Vice-Chair

ESSCIRC TPC

Bogdan Staszewski (University College Dublin, IE)	TPC Chair
Witold Pleskacz (WUT, PL)	TPC Co-Chair
Andreia Cathelin (STMicroelectronics, FR)	TPC Vice-Chair

TUTORIALS / WORKSHOPS

Grzegorz Deptuch (FNAL, US)	Co-Chair
Wladek Grabinski (GMC, CH)	Co-Chair
Piotr Grabiec (Institute of Electron Tech, PL)	Co-Chair
Wieslaw Kuzmicz (WUT, PL)	Co-Chair

ESSDERC/ESSCIRC STEERING COMMITTEE

Mikael Östling (KTH, SE)	Chair
Qiuting Huang (ETH Zurich, CH)	Vice-chair
Cor Claeys (KU Leuven, BE)	Exec. Secret.
Joachim Burghartz (IMS-Chips, DE)	
Wim Dehaene (KU Leuven, BE)	
Barbara De Salvo (Leti, FR)	
Tibor Grasser (Vienna University of Technology, AT)	
Joachim Knoch (RWTH Aachen, DE)	
Christoph Kutter (Fraunhofer EMFT, Munich, DE)	
Domine Leenaerts (NXP, NL)	
Andrea Mazzanti (University Pavia, IT)	
Thomas Mikolajick (Namlab, DE)	
Paolo Pavan (University of Modena and Reggio Emilia, IT)	
Stefan Rusu (TSMC, US)	
Christoph Sandner (Infineon, AT)	
Michiel Steyaert (KU Leuven, BE)	
Roland Thewes (TU Berlin, DE)	
Akira Toriumi (Tokyo University, JP)	

CONTACT

LOCAL SCIENTIFIC SECRETARIAT

Krzysztof Kasinski (AGH UST, PL)
Robert Szczygiel (AGH UST, PL)

ORGANIZING SECRETARIAT

Fundacja dla AGH | www.fundacja.agh.edu.pl
ul. Czarnowiejska 50B, 30-054 Cracow, Poland,
+48 12 617 46 04 | kf@agh.edu.pl

CRACOW - THE CITY OF KINGS

The magical city of Cracow is the second largest city in Poland. Located in the south of the country on the Vistula river, it is a capital city of Lesser Poland Voivodeship. It is a place where history and tradition intertwine with culture, modern technologies and economic development.

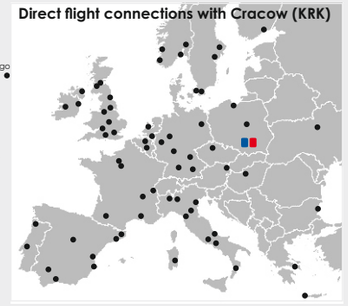
Officially rooted in XIIIth century, its history is much older. Being the capital of the Crown of the Kingdom of Poland between 1038 and 1569, it has never stopped thriving as an economic and cultural center. Cracow's Golden Age came by the end of the 15th century when it was the thriving metropolis of a vast and prosperous kingdom stretching from the Black Sea to the Baltic Sea.

The uniqueness of this place has not gone unnoticed. Entire Cracow's Historic Centre (Old Town) is on the UNESCO World Heritage List. It is recognized by many by its largest medieval market square in Europe and its architecture originating from Gothic through Renaissance and Baroque epochs. The Royal Wawel Castle, the seat of Polish kings and their biggest necropolis, is a diamond that rules over the landscape of the city. It was officially recognized as European Capital of Culture (2000), UNESCO City of Literature (2012) and hosted World Youth Days (2016) as well as participated in European Football Championship (2012).

Another important feature of Cracow is its academical prowess. With over 650 years of academic tradition, it holds one of the oldest civil universities in Europe (Jagiellonian University). Currently it is a home to five major universities (with AGH University of Science and Technology leading in engineering research) and various higher education school, which gives a total population of approximately 200 thousand students.

The high-tech landscape in Cracow continues to expand. It boast a special economic zone (Cracow Technological Park for major high-tech investments) with several major R&D centers (e.g. Motorola, ABB, Nokia, Aptiv, Silicon Creations, Ericsson, Comarch) focused on industrial electronics and software, four enterprise incubators, three commercial-fair grounds, and seven higher schools of economics. Over 100,000 private businesses and nearly 2,000 public firms carry on in Cracow with an aggregate revenue to the tune of 14.6 billion euro. Surprisingly, the city's big companies with hundreds and thousands on the payroll come under the spotlight yet they are hardly representative of Cracow's economy. The self-employed and small enterprises employing less than ten workers account for over ninety percent of business entities incorporated in the city. Foreigners own (wholly or partially) more than 1,900 of Cracow's companies."

Direct flight connections with Cracow (KRK)



CALL for PAPERS

IEEE SSCS ELECTRON DEVICES SOCIETY

WWW.ESSCIRC-ESSDERC2019.ORG

AGH Warsaw University of Technology CEZAMAT JAGIELLONIAN UNIVERSITY IN KRAKÓW

GENERAL PURPOSE OF THE CONFERENCE

The aim of **ESSDERC** and **ESSCIRC** is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary. While keeping separate Technical Program Committees, **ESSDERC** and **ESSCIRC** are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

CONFERENCE TOPICS

Although not limited, papers are solicited for the following main topics:

ESSDERC

CMOS Devices and Technology

CMOS scaling; Novel MOS device architectures; Circuit/device interaction and co-optimization; High-mobility channel devices; CMOS front-end or back-end processes; Interconnects; Integration of RF or photonic devices; 3D integration; Front-end and back-end manufacturing processes; 3D integration and wafer-level packaging; Reliability and characterization of materials, processes and devices; Advanced interconnects; ESD, latch-up, soft errors, noise and mismatch behavior, hot carrier effects, bias temperature instabilities, and EMI; Defect monitoring and control; Metrology; Test structures and methodologies; Manufacturing yield modeling, analysis and testing.

Opto-, Power and Microwave Devices

New device or process architectures; New phenomena and performance improvement of optoelectronic, high voltage, smart power, IGBT, microwave devices; Passive devices, antennas and filters (including Si, Ge, SiC, GaN); Optoelectronic devices including sensors, LEDs, semiconductor lasers; Photovoltaic devices; Studies of high temperature operation; IC cooling and packaging aspects; Reliability and characterization of materials, processes and devices.

Physical Modeling of Materials and Devices

Numerical, analytical and statistical modeling and simulation of electronic, optical or hybrid devices, the interconnect, isolation and 2D or 3D integration; Aspects of materials, fabrication processes and devices, e.g. advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport, and other related aspects); Mechanical or electro-thermal modeling and simulation; DfM. Reliability of materials and devices.

Compact Modeling of Devices and Circuits

Compact/SPICE modeling of electronic, optical, organic, and hybrid devices and their IC implementation and interconnection. Topics include compact/SPICE models and their Verilog-A standardization of the semiconductor devices (including Bio/Med sensors, MEMS, Microwave, RF, High voltage and Power), parameter extraction, compact models for emerging technologies and novel devices, performance evaluation, reliability, variability, and open source benchmarking/implementation methodologies. Modeling of interactions between process, device, and circuit design as well as Foundry/Fabless Interface Strategies.

Memory Devices and Technology

Embedded and stand-alone memories; DRAM, FeRAM, MRAM, ReRAM, PCRAM, Flash, Nanocrystal and single/few-electron memories, Organic memories, NEMS-based devices, Selectors; Novel memory cell concepts and architectures, covering device physics, reliability, process integration and manufacturability issues and including 3D NAND Flash, crosspoint arrays, and 3D systems integration; Devices and concepts for neuromorphic computing, memory-enabled logic and security applications.

Emerging non-CMOS Devices and Technologies

Novel non-CMOS materials, processes and devices, (carbon-nanotubes, nanowires and nanoparticles, 2D materials, graphene, metal oxides, etc.) for electronic, optoelectronic, sensor & actuator applications; Reliability and characterization of materials, processes and devices; Molecular and quantum devices; Nanophotonics, plasmonics, spintronics, self-assembling methods; Energy harvesters; High frequency digital and analog devices including THz; New high-mobility channels (strained Si, Ge, SiGe).

Sensor Devices and Technology

Design, fabrication, modeling, reliability, packaging and smart systems integration of actuators (discrete SoC, SiP, or heterogenous 3D integration); MEMS, NEMS, optical, chemical or biological sensors; Display technologies; High-speed imagers; TFTs; Organic and flexible substrate electronics.

ESSCIRC

Analog

OP-Amps and instrumentation amplifiers; CT and DT filters; SC circuits, Comparators; Voltage and current references; High voltage circuits; Nonlinear analog circuits; Digitally assisted analog circuits.

Data Converters

Nyquist-rate and oversampling A/D and D/A converters; Sample-hold circuits; Time-to-digital converters; ADC and DAC calibration/error correction circuits.

RF and mm-Wave

RF/IF building blocks like LNAs, mixers, power amplifiers, IF amplifiers; Power detectors; Subsystems for RF, mm-wave and THz design.

Frequency Generation

Modulators/demodulators; VCOs; PLLs; DLLs; Frequency synthesizers; Frequency dividers; Integrated passive components.

Wireless and Wireline Systems

Receivers/transmitters/transceivers for wireless/wireline systems Gigabit serial links; Clock and data recovery; Equalization; Advanced modulation systems; Base station and handset applications; TV/radio/satellite receivers and transmitters; Radars.

Sensors, Imager and Biomedical

Sensor subsystems and interfaces; Accelerometers; Temperature sensing; Imaging and smart imaging chips; AMOLED; MEMs subsystems; RF MEMs; Implantable electronic ICs; Biomedical imagers; Bio-MEMs integrated systems; Lab-on-chip; Organic LED and liquid-crystal-display interface circuits; Flat panel and projection display.

Digital, Security and Memory

Techniques for energy efficient and high performance digital circuits; I/O and inter-chip communication; Reconfigurable digital circuits; Security and encryption circuits; Clocking; Arithmetic building blocks; Memories; Microprocessors; DSPs; Memory interfacing; Bus interfacing; Many core and multirate ICs; 3D integration.

Power Management

Energy transducers; Power regulators; DC-DC converters; Energy-scavenging circuits; LDOs Boost-buck-converters; LED and gate drivers; Sequencers and supervisors; Green circuits.

PAPER SUBMISSION

Manuscript guidelines as well as instructions on how to submit electronically will be available on the conference website. Papers must not exceed four A4 pages with all illustrations and references included.

All submissions must be received by 8th April 2019.

Papers submitted for review must clearly state:

- The purpose of the work
- How and to what extent it advances the state-of-the art
- Specific results and their impact

Only work that has not been previously published or submitted elsewhere will be considered.

Submission of a paper for review and subsequent acceptance is considered as a commitment that the work will not be publicly available prior to the conference.

After selection of papers, the authors will be informed about the decision of the Technical Program Committee by e-mail by 31th May 2019.

At the same time, the complete program will be published on the conference website. An oral presentation will be given at the Conference for each accepted paper. No-shows will result in the exclusion of the papers from any conference related publication. The submitted final PDF files should be IEEE Xplore compliant.

For each paper independently, at least one co-author is required to register for the Conference (one registration-one paper policy).

Registration fees and deadlines will be available on the conference website.